美浦森半导体
M s e m i t e k

Halogen Free

RoHS LEAD FREE

SLD80R830GT

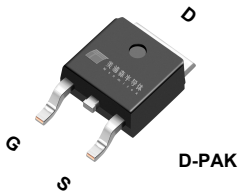
800V N-Channel Multi-EPI Super-JMOSFET

General Description

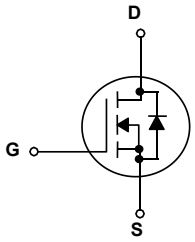
This Power MOSFET is produced using Msemitek's advanced Superjunction MOSFET technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies.

Features

- 850V@T_j=150℃
- 6A,800V, $R_{DS(on)}$ =740mΩ@V_{GS} = 10 V
- Low gate charge(typ. Qg =17.7nC)
- High ruggedness
- Ultra fast switching
- 100% avalanche tested
- Improved dv/dt capability



D-PAK



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	SLD80R830GT	Units
V_{DSS}	Drain-Source Voltage	800	V
I_D	Drain Current * - Continuous (T_C = 25℃)	6	A
	- Continuous (T_C = 100℃)	3.8	A
I_{DM}	Drain Current * - Pulsed (Note 1)	18	A
V_{GSS}	Gate-Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	14	mJ
P_D	Power Dissipation (T_C = 25℃)	125	W
	- Derate above 25℃	1.0	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	260	℃

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	SLD80R830GT	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.0	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	℃/W

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLD80R830GT	SLD80R830GT	TO-252	Tape & Reel	2500	25000

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	800	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V	--	--	1	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	-100	--	--	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.5	--	4.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 3A	--	740	850	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} =100 V, V_{GS} = 0 V, f = 100KHz	--	611	--	pF
C_{oss}	Output Capacitance		--	186	--	pF
C_{rss}	Reverse Transfer Capacitance		--	0.9	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 400V, I_D = 6A, R_G = 4.7Ω, V_{GS} = 10V (Note3)	--	10	--	ns
t_r	Turn-On Rise Time		--	33	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	30	--	ns
t_f	Turn-Off Fall Time		--	28	--	ns
Q_g	Total Gate Charge	V_{DS} =400V, I_D = 6A, V_{GS} =10V (Note3)	--	17.7	--	nC
Q_{gs}	Gate-Source Charge		--	2.8	--	nC
Q_{gd}	Gate-Drain Charge		--	6.1	--	nC
R_G	Gate Resistance	f =1MHz	--	6.3	--	Ω
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	6	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	18	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 6A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{DS} =400 V, I_S = 6A, dI_F / dt = 100A/us	--	248	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.4	--	uC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T_J =25℃, V_{DD} =50V, V_G =10V, L=10mH,
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Characteristics

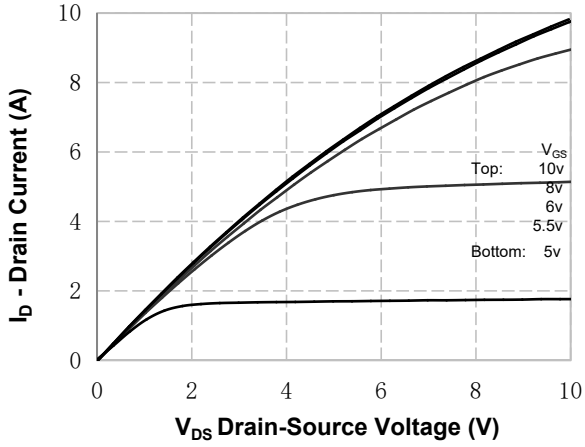


Figure 1. On-Region Characteristics

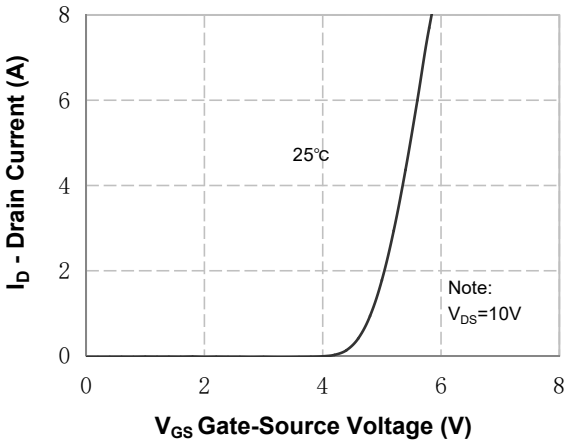


Figure 2. Transfer Characteristics

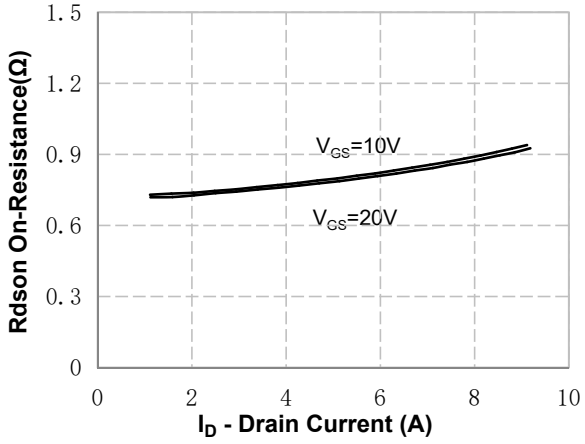


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

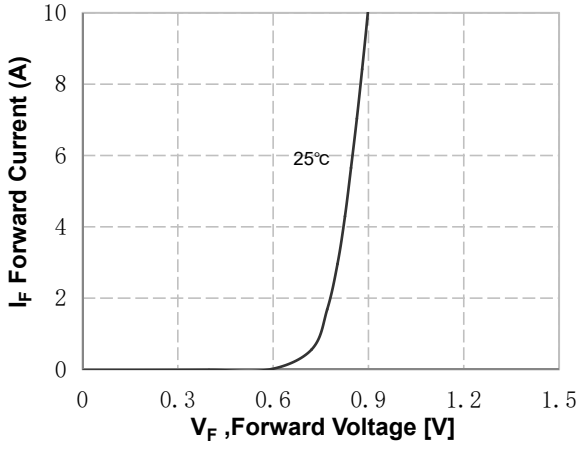


Figure 4. Body Diode Forward Voltage Variation with Source Current

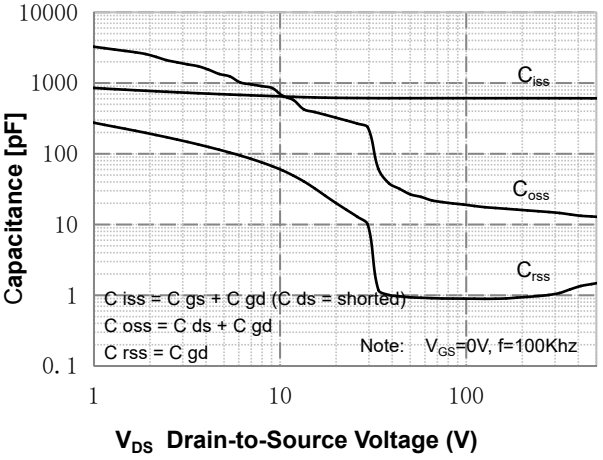


Figure 5. Capacitance Characteristics

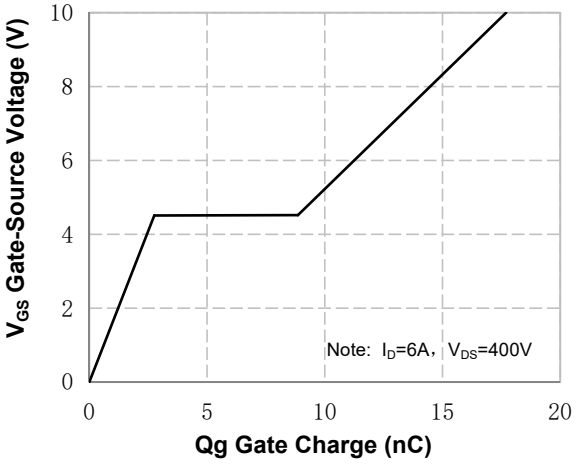


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

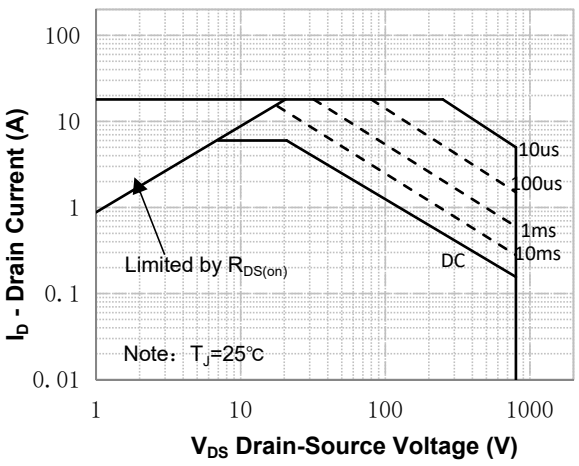


Figure 7. Maximum Safe Operating Area

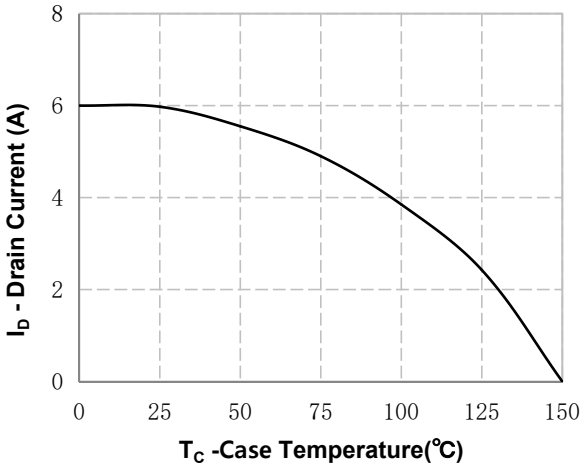


Figure 8. Maximum Drain Current vs Case Temperature

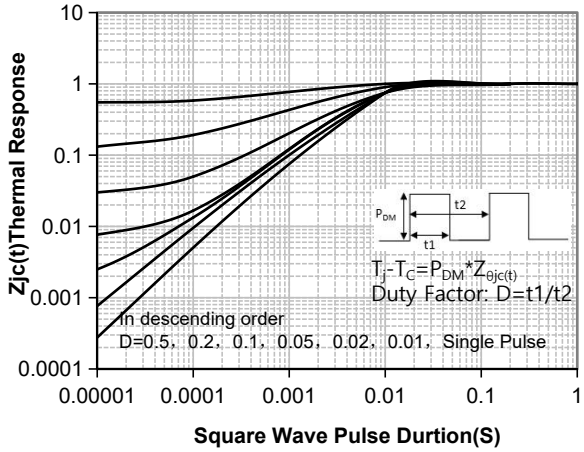
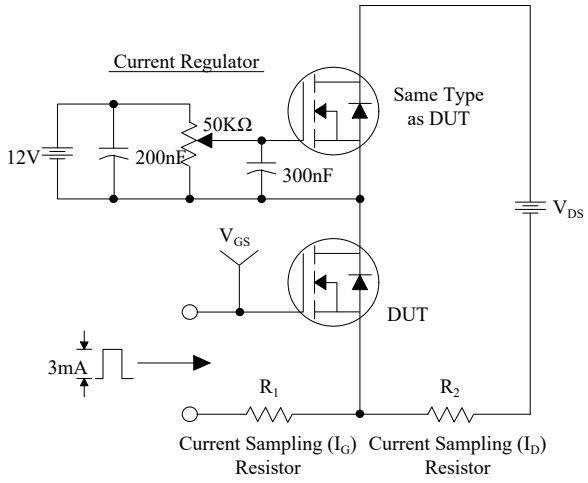
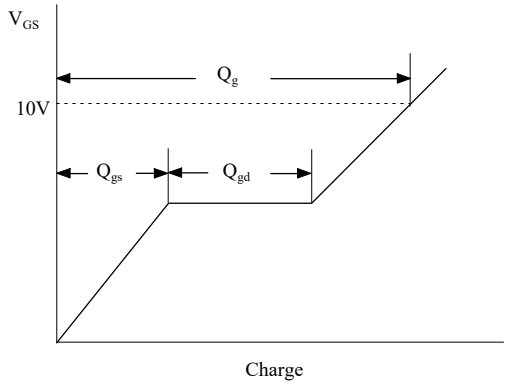


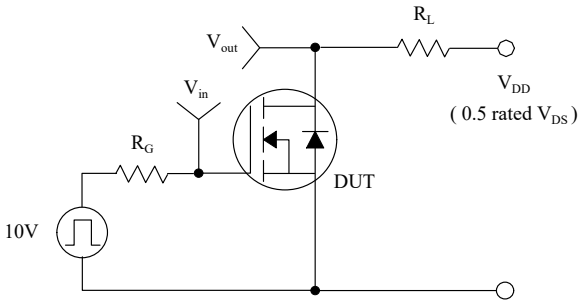
Figure 9. Transient Thermal Response Curve

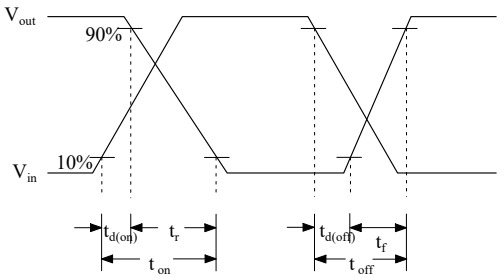
Gate Charge Test Circuit & Waveform



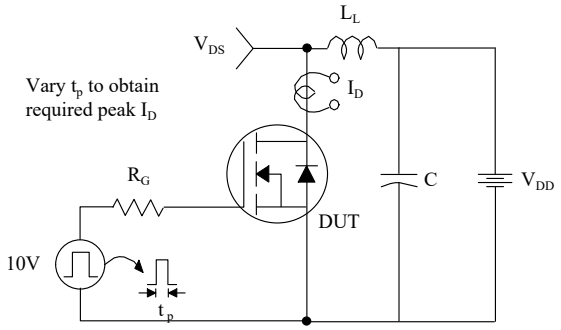


Resistive Switching Test Circuit & Waveforms

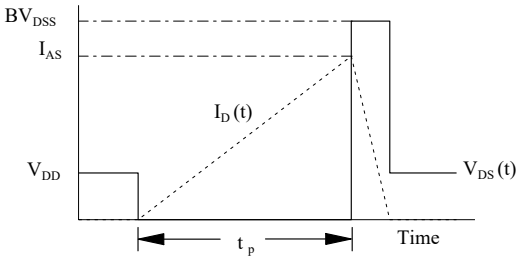




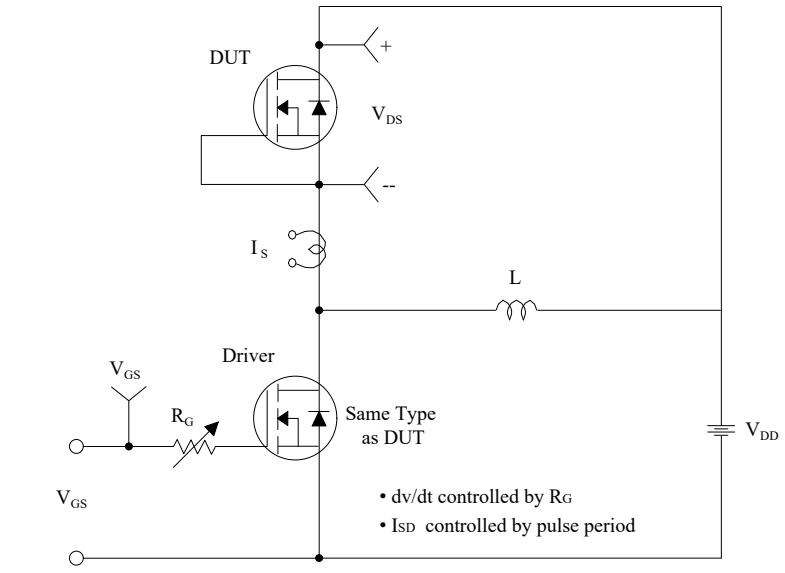
Unclamped Inductive Switching Test Circuit & Waveforms

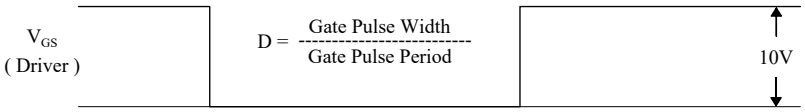


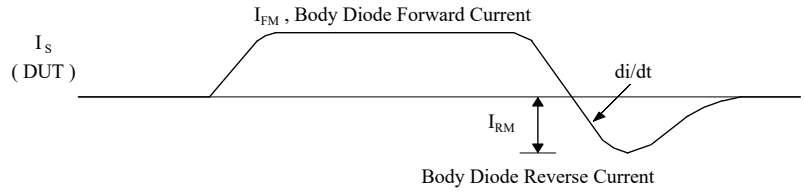
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

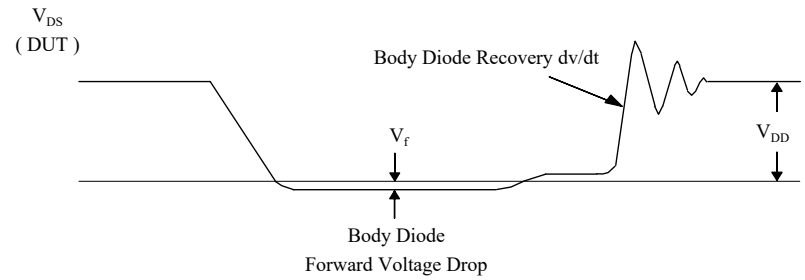


Peak Diode Recovery dv/dt Test Circuit & Waveforms

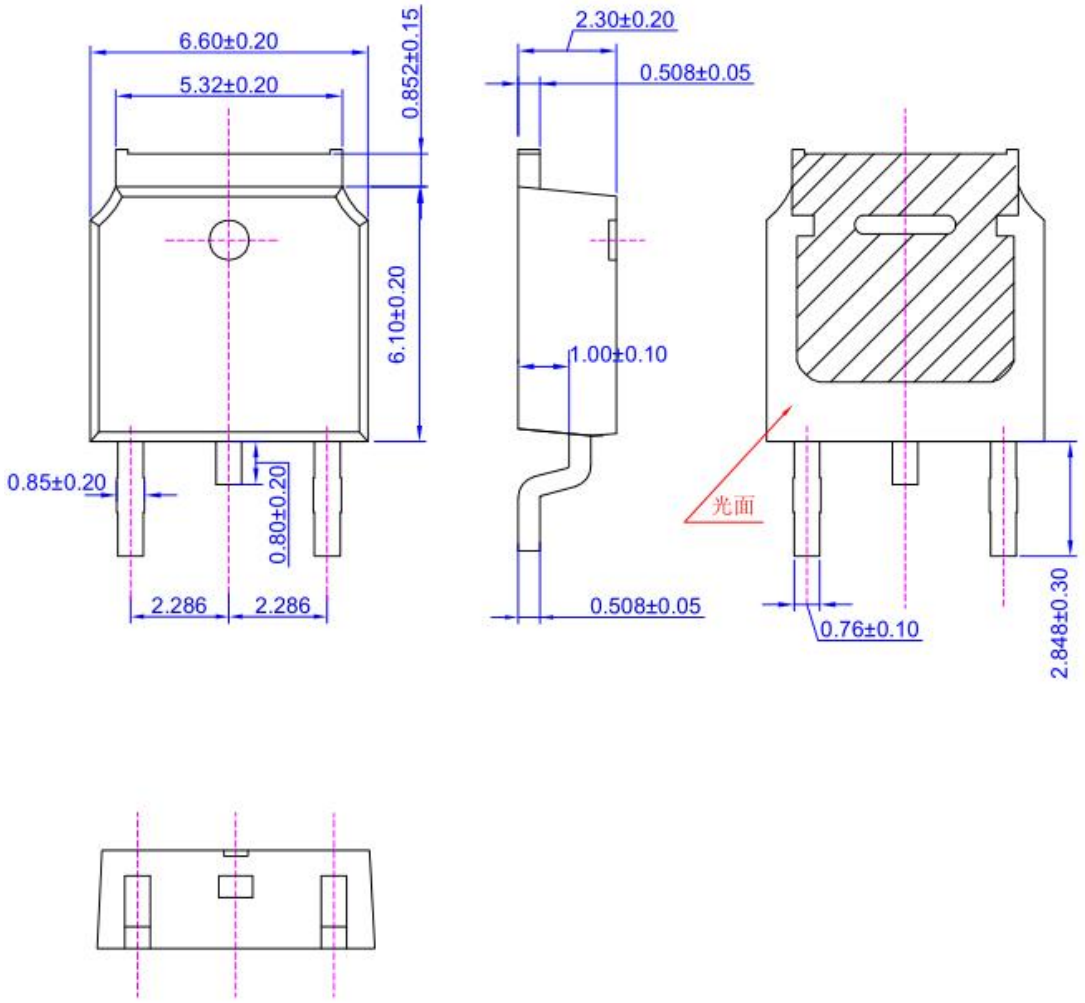








TO-252 OUTLINE



NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25

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