

# SLD65R420E7

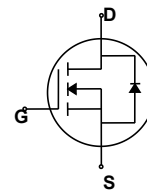
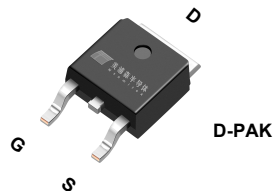
## 650V N-Channel Multi-EPI Super-JMOSFET

### General Description

This Power MOSFET is produced using Msemitek's advanced Superjunction MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies.

### Features

- 11A, 650V,  $R_{DS(on)typ} = 0.318\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 15.5nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	SLD65R420E7	Units
$V_{DSS}$	Drain-Source Voltage	650	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	11	A
		7	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	28.8	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
EAS	Single Pulsed Avalanche Energy (Note 2)	246	mJ
$I_{AR}$	Avalanche Current (Note 1)	11	A
$E_{AR}$	Repetitive Avalanche Energy	6.25	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
	MOSFET dv/dt	100	
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	87	W
		0.7	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

\* Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	SLD65R420E7	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.43	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C}/\text{W}$

## Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLD65R420E7	SLD65R420E7	D-Pak	Tape & Reel	5000	25000

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	650	--	--	V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 150^\circ\text{C}$	650	--	--	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	uA
		$V_{DS} = 520\text{ V}, T_C = 125^\circ\text{C}$	--	2	--	uA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 0.8\text{ mA}$	2.5	--	4.5	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.0\text{ A}$	--	318	420	mΩ
R <sub>G</sub>	Gate resistance	F=1MHZ	--	1.0	--	Ω

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	--	920	--	pF
C <sub>oss</sub>	Output Capacitance		--	20	--	pF
C <sub>o(tr)</sub>	Time Related Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	--	239	--	pF
C <sub>o(er)</sub>	Energy Related Output Capacitance		--	30	--	pF

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 4.0\text{ A},$ $R_G = 10\ \Omega$  (Note 4, 5)	--	8	--	ns
t <sub>r</sub>	Turn-On Rise Time		--	13	--	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	30	--	ns
t <sub>f</sub>	Turn-Off Fall Time		--	8	--	ns
Q <sub>g</sub>	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 4.0\text{ A},$ $V_{GS} = 10\text{ V}$  (Note 4, 5)	--	15.5	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	3.0	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	7.9	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	--	--	9.6	A	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current	--	--	28.8	A	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 4.0\text{ A}$	--	--	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{DD} = 400\text{ V}, I_S = 4.0\text{ A},$ $dI_F / dt = 100\text{ A/us}$ (Note 4)	--	221	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	1.8	--	uC

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 79 mH, I<sub>AS</sub> = 2.5A, V<sub>DD</sub> = 100V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 4A, di/dt ≤ 100A/us, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test : Pulse width ≤ 300us, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

### Typical Characteristics

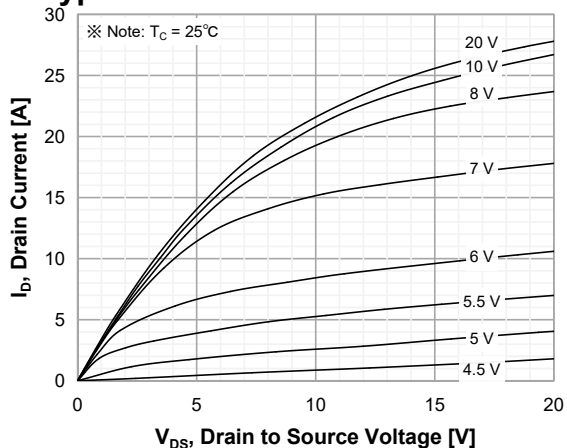


Figure 1. On-Region Characteristics

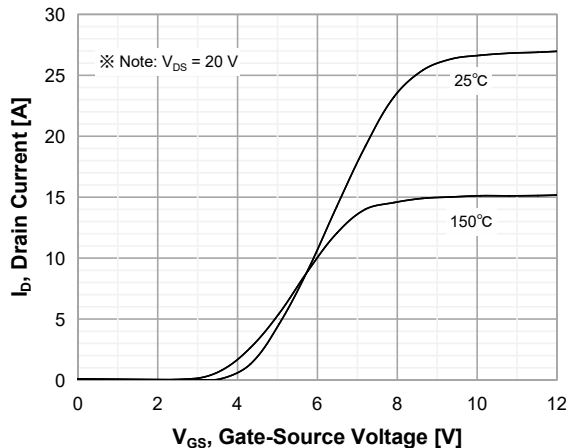


Figure 2. Transfer Characteristics

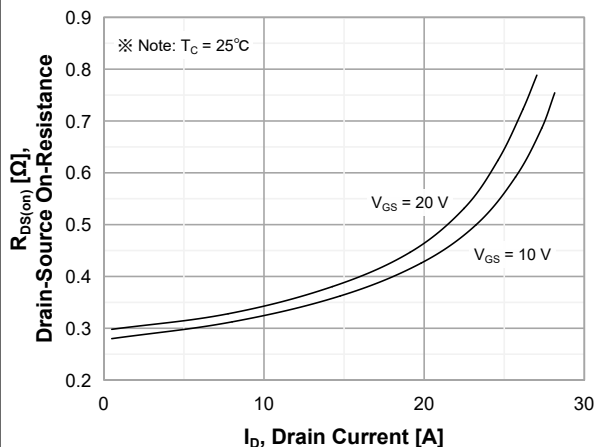


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

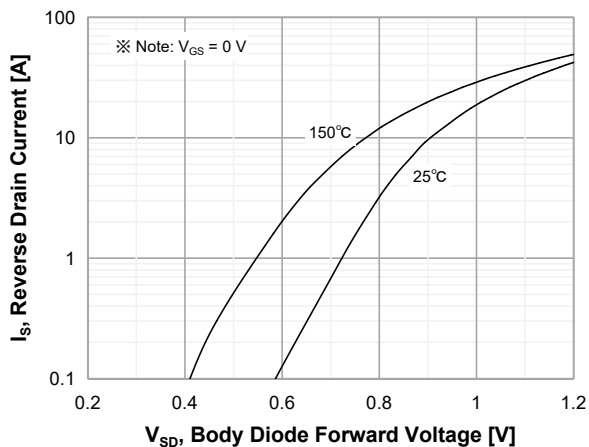


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

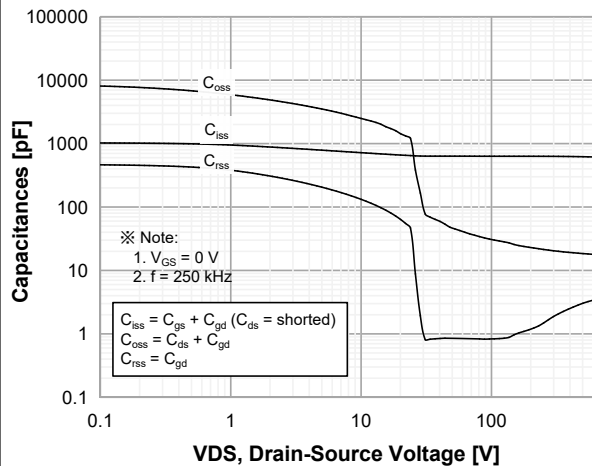


Figure 5. Capacitance Characteristics

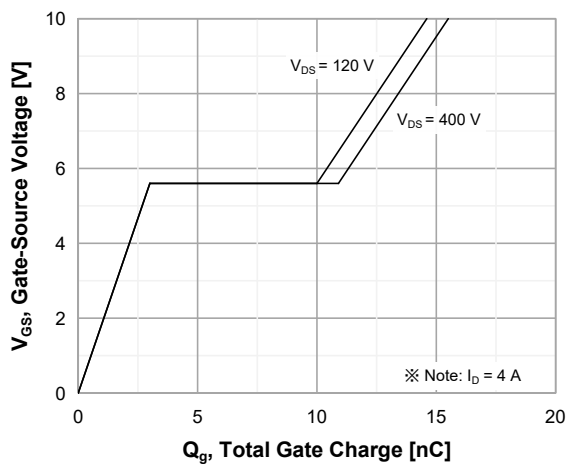


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

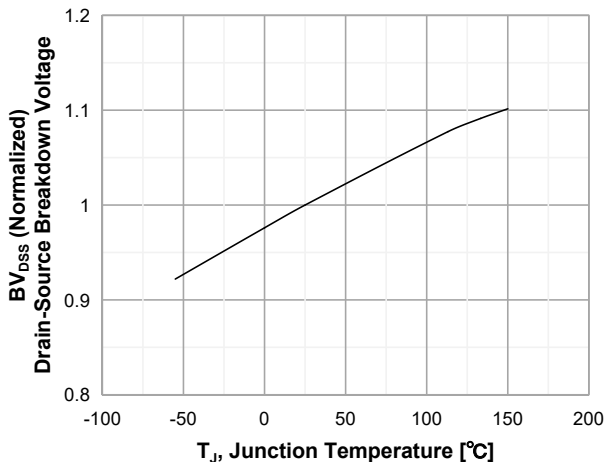


Figure 7. Breakdown Voltage Variation vs Temperature

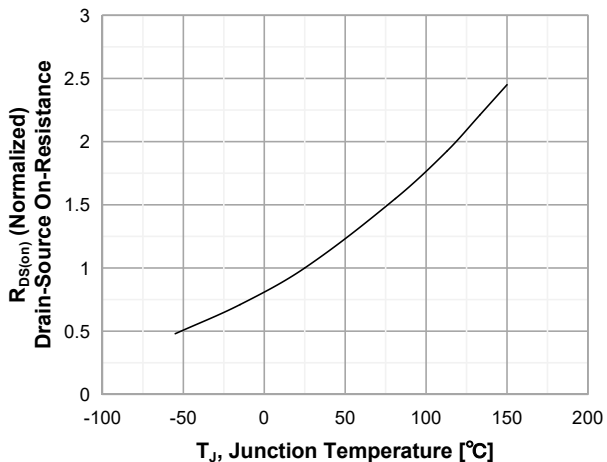


Figure 8. On-Resistance Variation vs Temperature

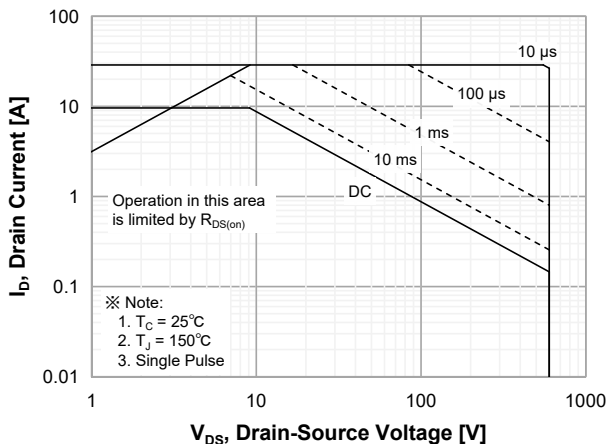


Figure 9. Maximum Safe Operating Area

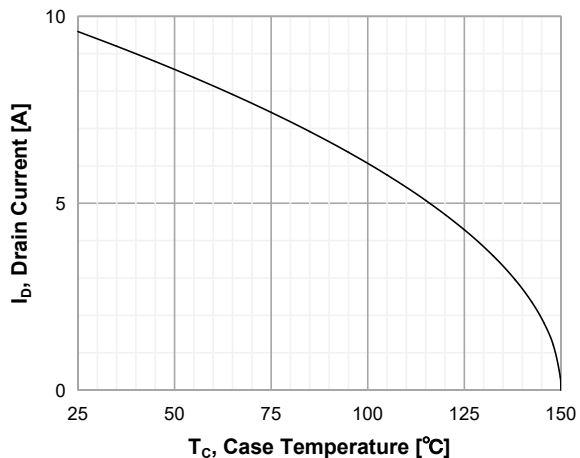


Figure 10. Maximum Drain Current vs Case Temperature

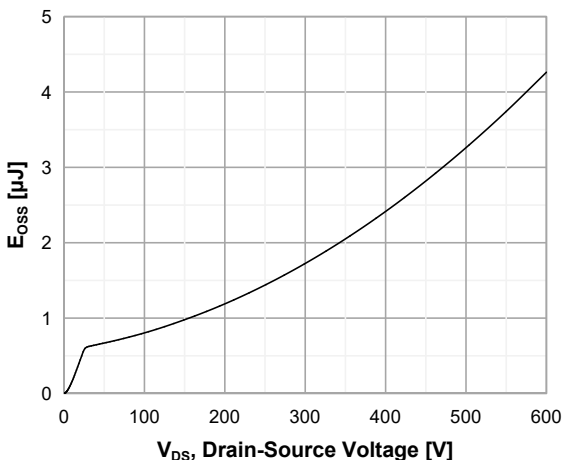


Figure 11.  $E_{OSS}$  vs. Drain to Source Voltage

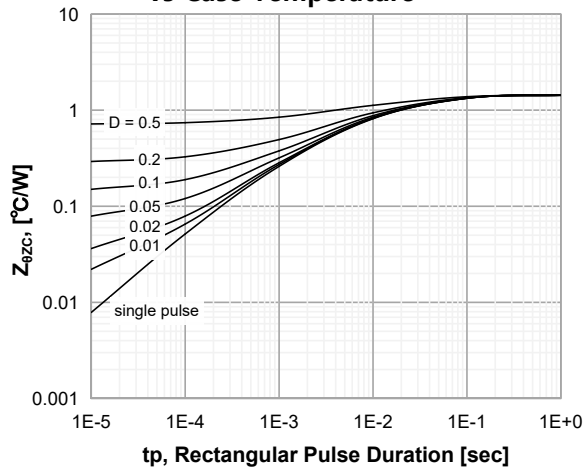
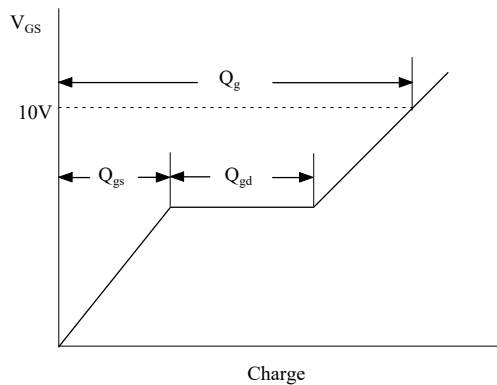
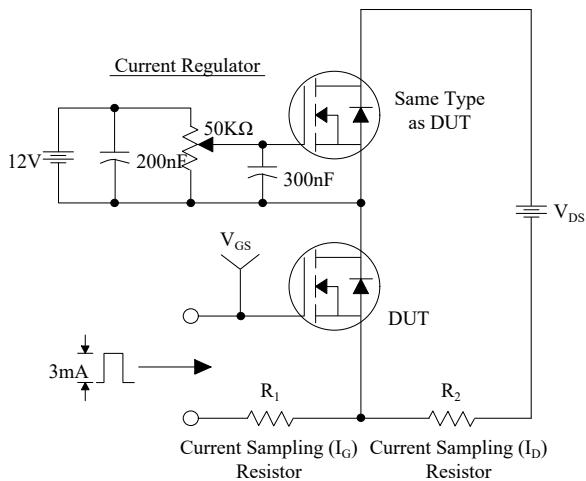
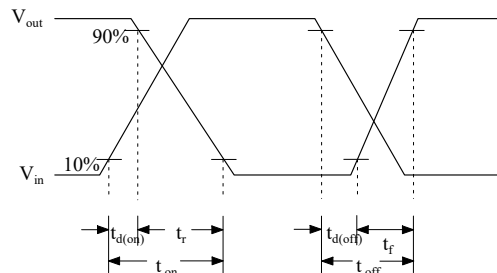
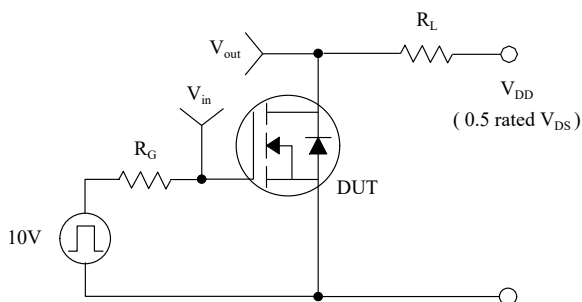


Figure 12. Transient Thermal Response Curve

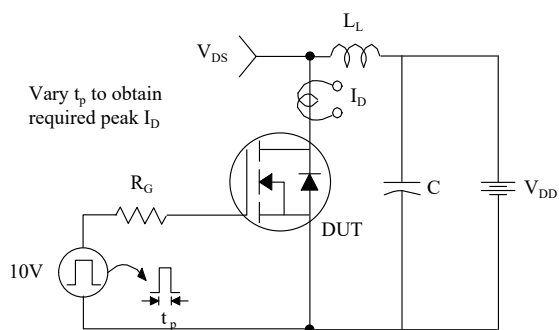
### Gate Charge Test Circuit & Waveform



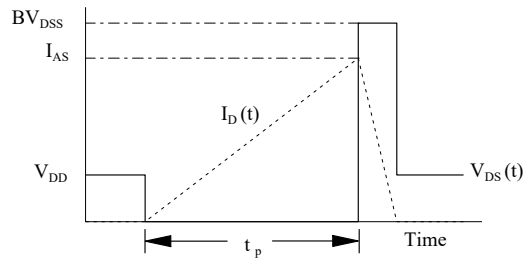
### Resistive Switching Test Circuit & Waveforms



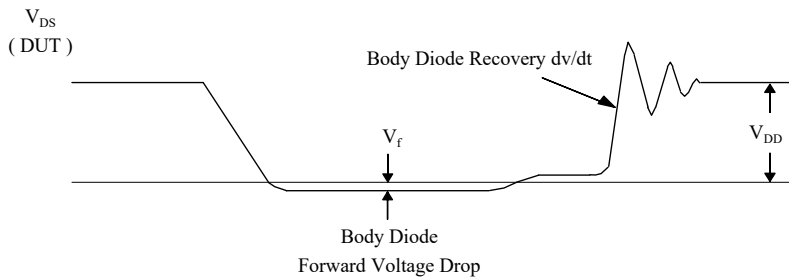
### Unclamped Inductive Switching Test Circuit & Waveforms



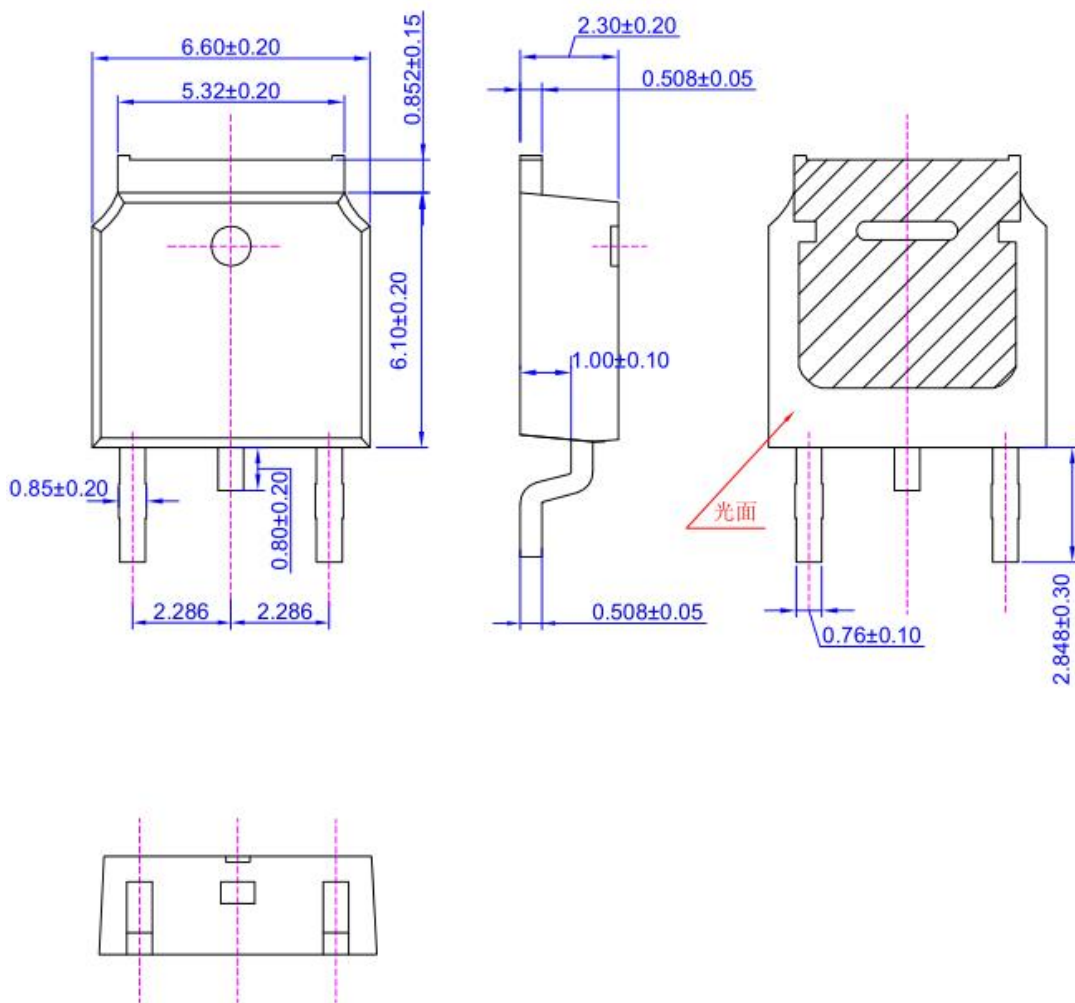
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



# Peak Diode Recovery dv/dt Test Circuit & Waveforms



## TO-252 OUTLINE



## NOTE:

- 1The plastic package is not marked as smooth surface  $R_a=0.1$ ; Subglossy surface  $R_a=0.8$
- 2.Undeclared tolerance  $\pm 0.25$ , Unmarked fillet  $R_{max}=0.25$

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