

# SLD30L03A

## N And P-Channel Enhancement Mode MOSFET

### General Description

This Power MOSFET is produced using Msemitek's advanced TRENCH technology.

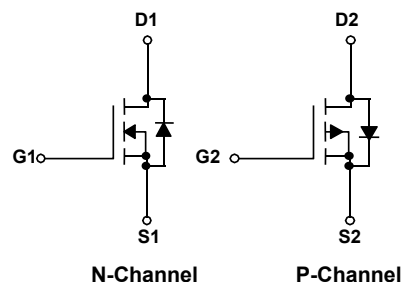
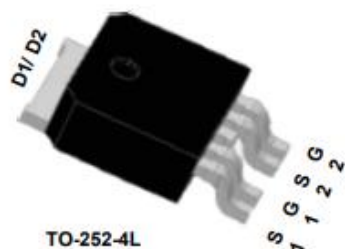
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

### Application

- Battery Protection
- Load Switch
- Power Management

### Features

- N-Channel: 30V 25A  
 $R_{DS(on)Typ} = 9m\Omega @ V_{GS} = 10V$   
 $R_{DS(on)Typ} = 13m\Omega @ V_{GS} = 4.5V$
- P-Channel: -30V- 20A  
 $R_{DS(on)Typ} = 23m\Omega @ V_{GS} = -10V$   
 $R_{DS(on)Typ} = 34.5m\Omega @ V_{GS} = -4.5V$
- Very Low On-resistance  $R_{DS(on)}$
- Low  $C_{rss}$
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
$V_{DSS}$	Drain-Source Voltage	30	-30	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ ) - Continuous ( $T_C = 100^\circ C$ )	25	-20	A
		14	-13	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	120	-60	A
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$P_D$	Power Dissipation ( $T_C = 25^\circ C$ )	15.5	27	W
$R_{\theta Jc}$	Thermal Resistance, Junction to Case	8	4.6	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ C$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ C$

\* Drain current limited by maximum junction temperature.

## Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLD30L03A	SLD30L03A	T0-252-4L	Tape	2500	25000

## N-Channel Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30	--	--	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 24\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	-	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	--	9	13	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	13	20	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 30\text{ A}$	--	15	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1116	-	pF
$C_{oss}$	Output Capacitance		--	187	-	pF
$C_{rss}$	Reverse Transfer Capacitance		--	152	-	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $R_L = 2.5\text{ }\Omega, I_D = 15\text{ A}$	--	15	--	ns
$t_r$	Turn-On Rise Time		--	19	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	--	ns
$t_f$	Turn-Off Fall Time		--	21	--	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 15\text{ A},$ $V_{GS} = 10\text{ V}$	--	13.3	--	nC
$Q_{gs}$	Gate-Source Charge		--	3.1	--	nC
$Q_{gd}$	Gate-Drain Charge		--	5	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	30	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	120	A

#### Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. Pulse Test: Pulse Width $\leq$ 300 $\mu\text{s}$ , Duty Cycle $\leq$ 2%

**P-Channel Electrical Characteristics** $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	-30	--	--	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -24\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.0	-	-2.2	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -10\text{ A}$	--	23	34	m $\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$	-	34.5	46	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -20\text{ A}$	--	18	--	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2800	-	pF
$C_{oss}$	Output Capacitance		--	346	-	pF
$C_{rSS}$	Reverse Transfer Capacitance		--	319	-	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = -10\text{ V}, V_{DS} = -15\text{ V},$ $R_L = 2.3\text{ }\Omega, I_D = -20\text{ A}$	--	14	--	ns
$t_r$	Turn-On Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	95	--	ns
$t_f$	Turn-Off Fall Time		--	65	--	ns
$Q_g$	Total Gate Charge	$V_{DS} = -15\text{ V}, I_D = -20\text{ A},$ $V_{GS} = -10\text{ V}$	--	30	--	nC
$Q_{gs}$	Gate-Source Charge		--	5.3	--	nC
$Q_{gd}$	Gate-Drain Charge		--	7.6	--	nC

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	-10	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-40	A

**Notes:**

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. Pulse Test: Pulse Widths $\leq$ 300 $\mu\text{s}$ , Duty Cycle $\leq$ 2%

### N- Channel Typical Characteristics

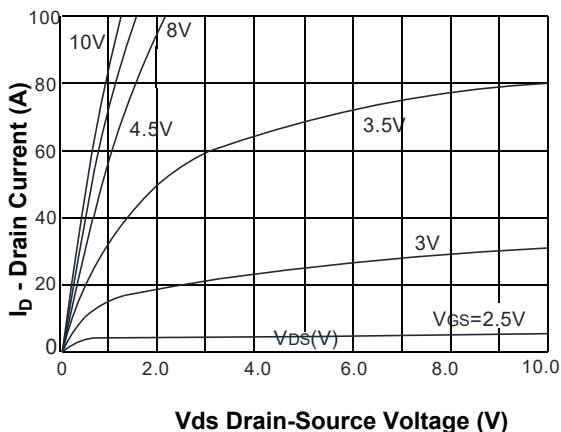


Figure 1. On-Region Characteristics

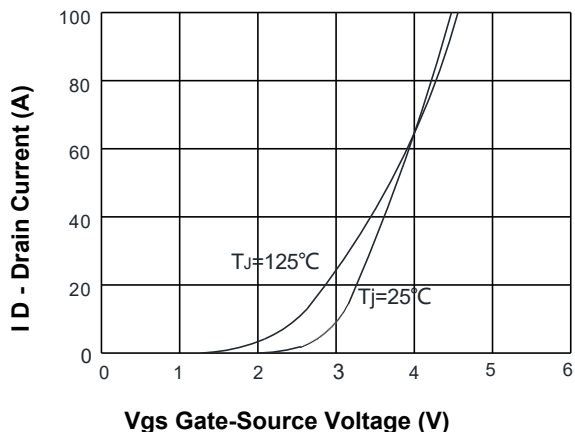


Figure 2. Transfer Characteristics

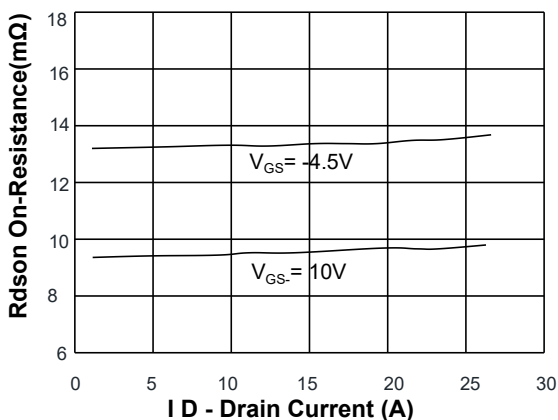


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

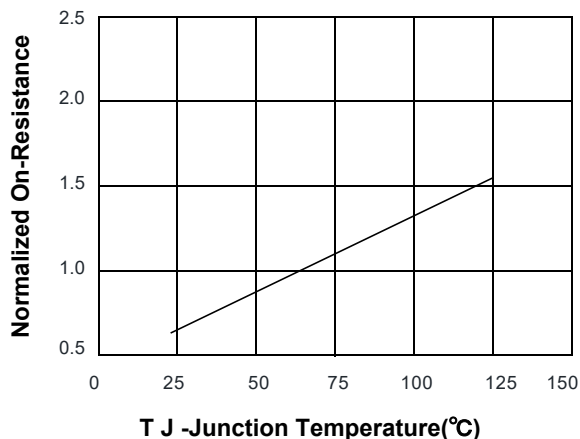


Figure 4. On-Resistance Variation vs Temperature

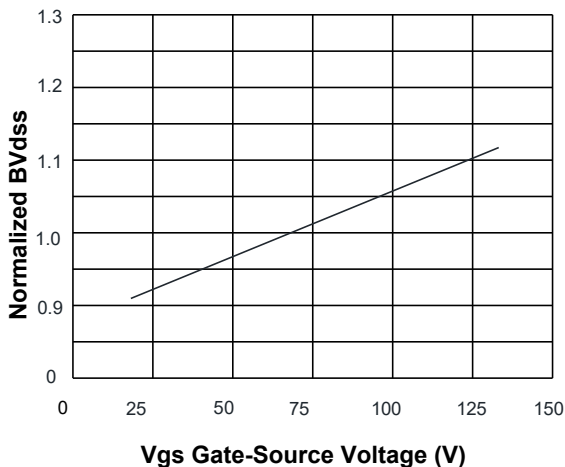


Figure 5. On-Resistance Variation vs Temperature

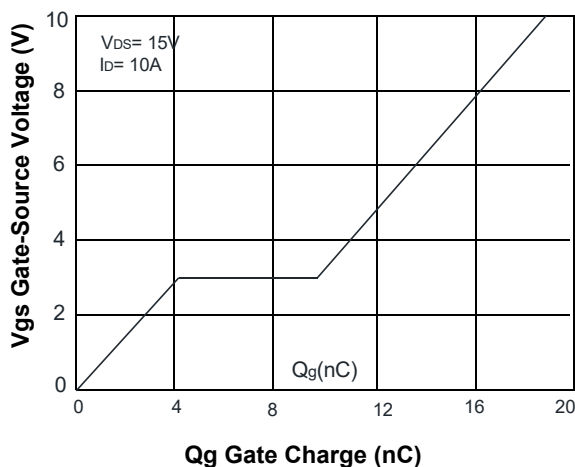


Figure 6. Gate Charge Characteristics

**N- Channel Typical Characteristics** (Continued)

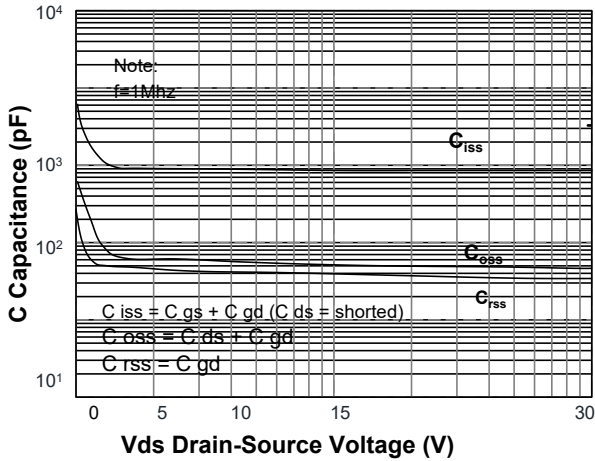


Figure 7. Capacitance vs Vds

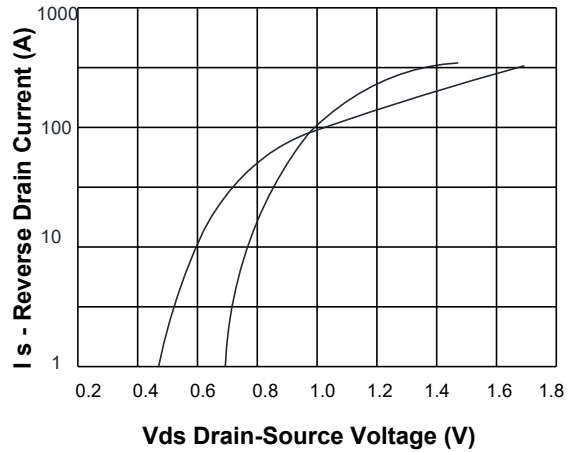


Figure 8. Reverse Drain Current vs Temperature

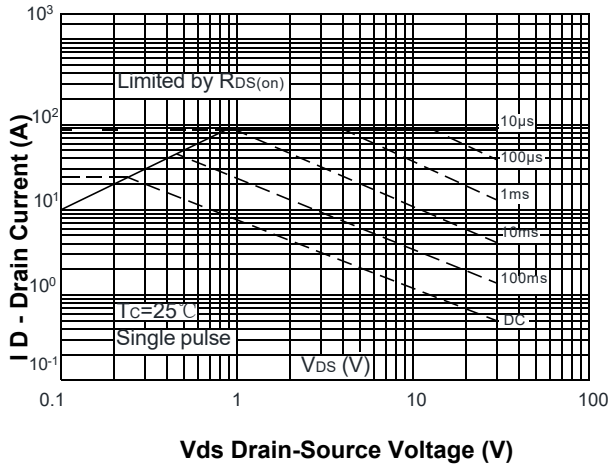


Figure 9. Maximum Safe Operating Area

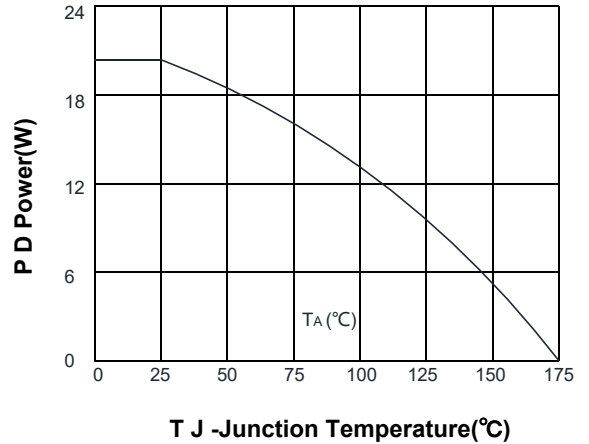


Figure 10. Maximum Power Dissipation vs Case Temperature

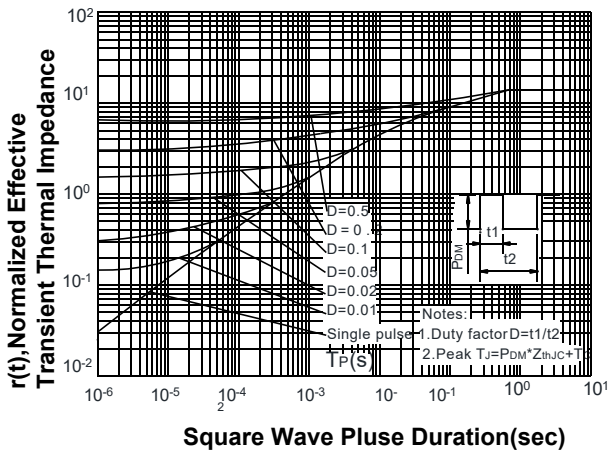


Figure 11. Transient Thermal Response Curve

### P- Channel Typical Characteristics

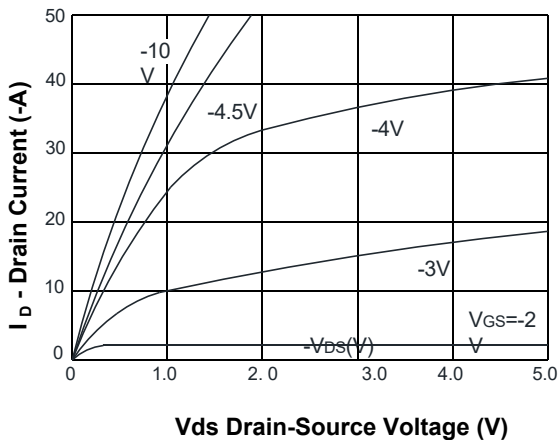


Figure 1. On-Region Characteristics

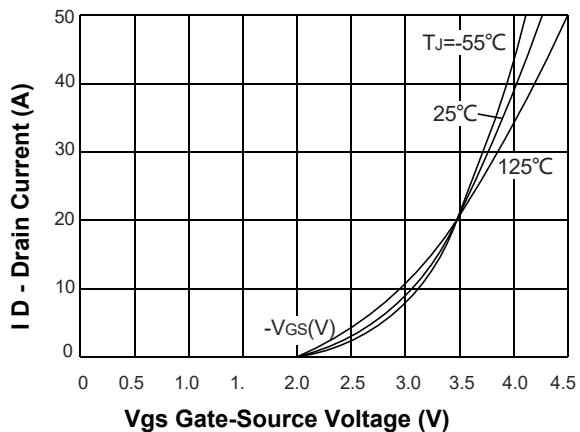


Figure 2. Transfer Characteristics

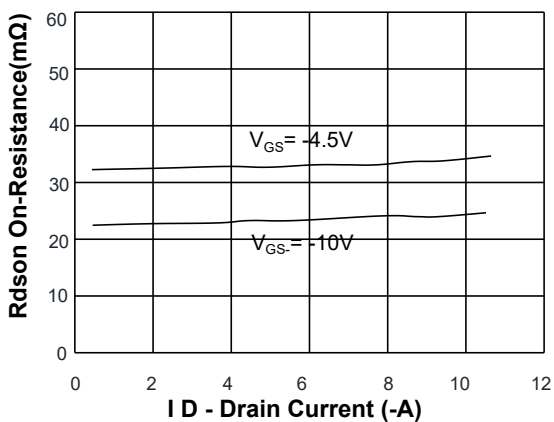


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

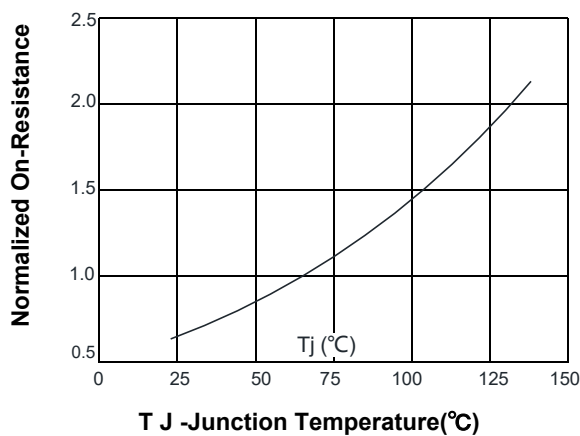


Figure 4. On-Resistance Variation vs Temperature

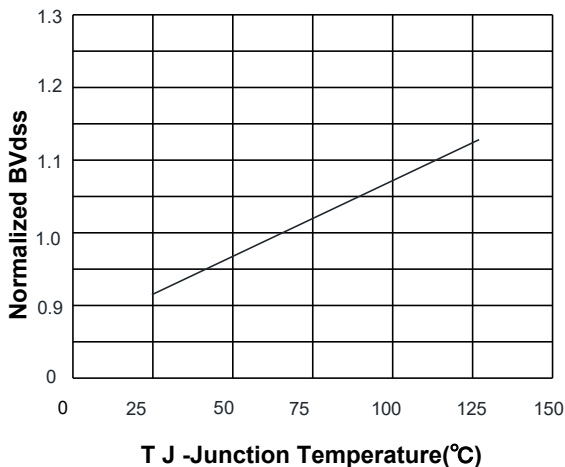


Figure 5. BV DSS vs Junction Temperature

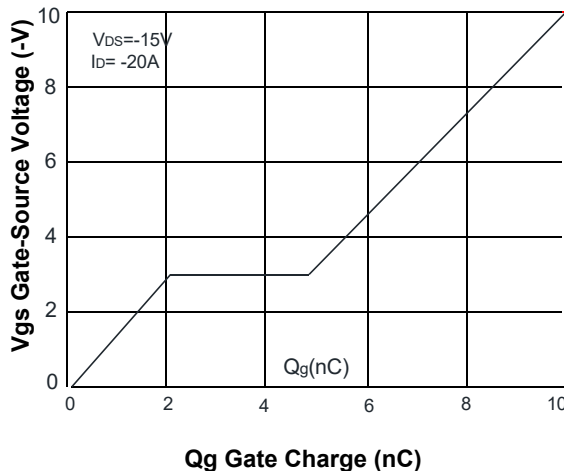


Figure 6. Gate Charge Characteristics

**P- Channel Typical Characteristics** (Continued)

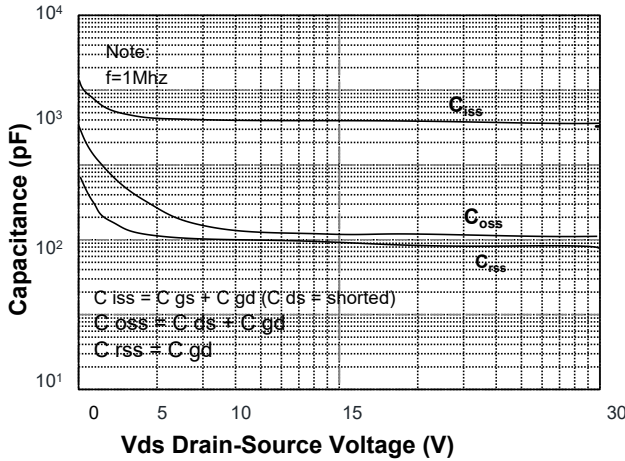


Figure 7. Capacitance vs Vds

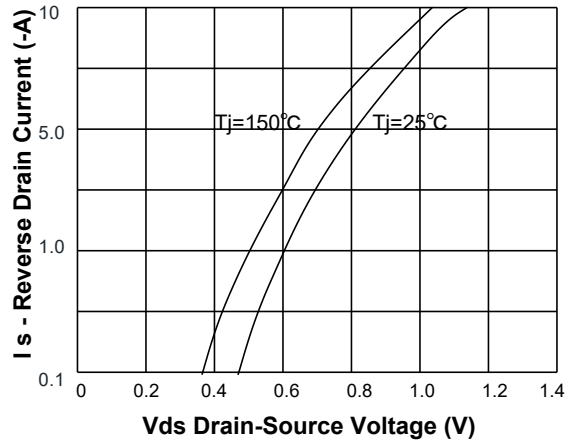


Figure 8. Reverse Drain Current vs Temperature

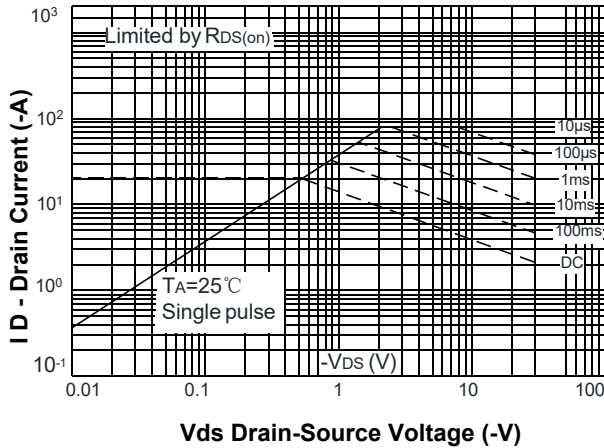


Figure 9. Maximum Safe Operating Area

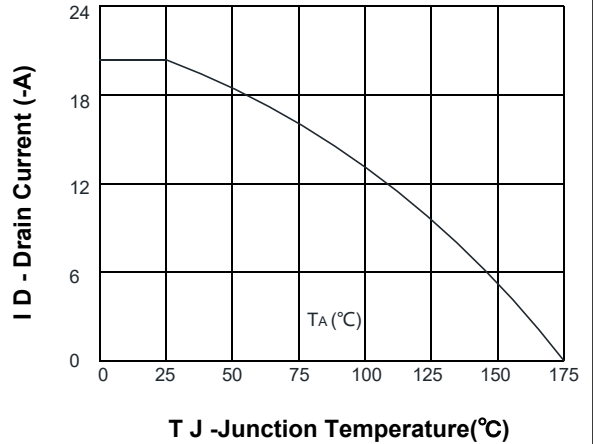


Figure 10. Maximum Drain Current vs Case Temperature

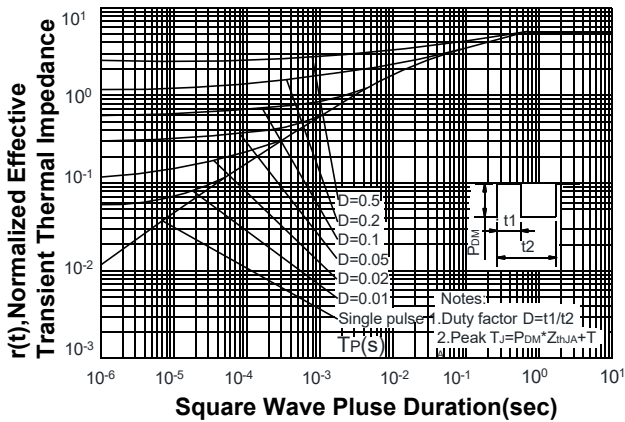
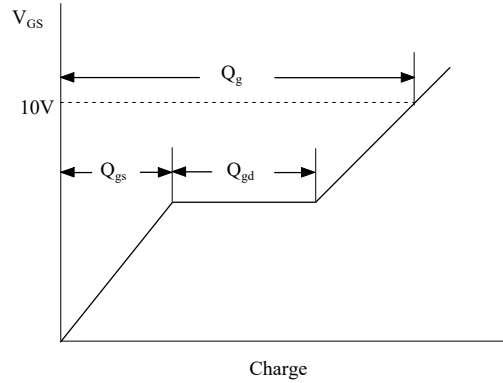
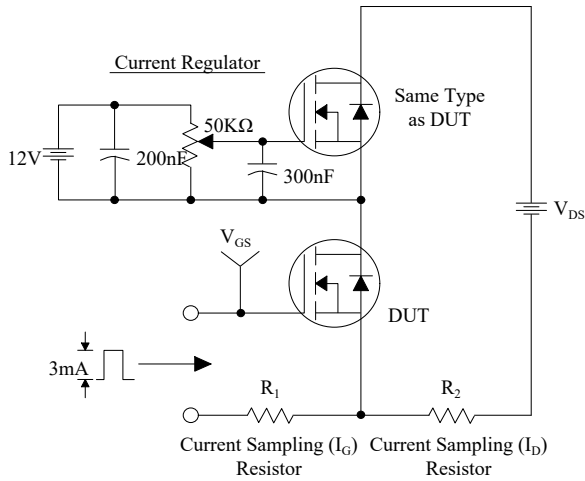
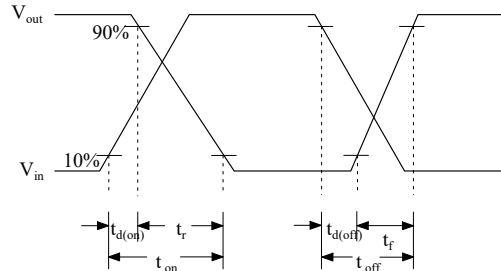
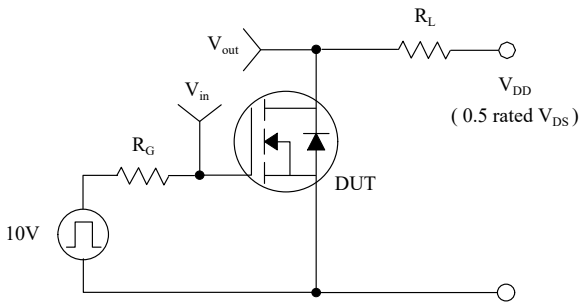


Figure 11. Transient Thermal Response Curve

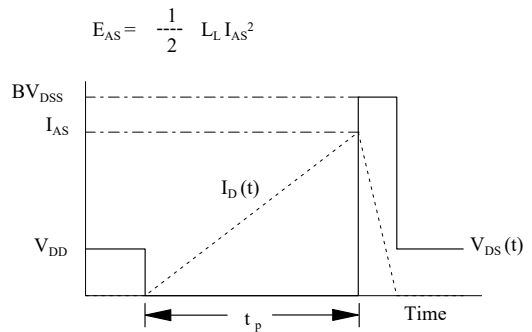
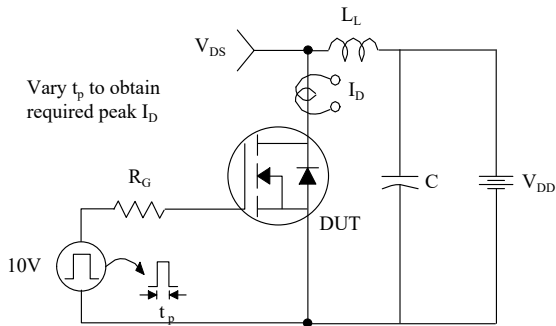
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms

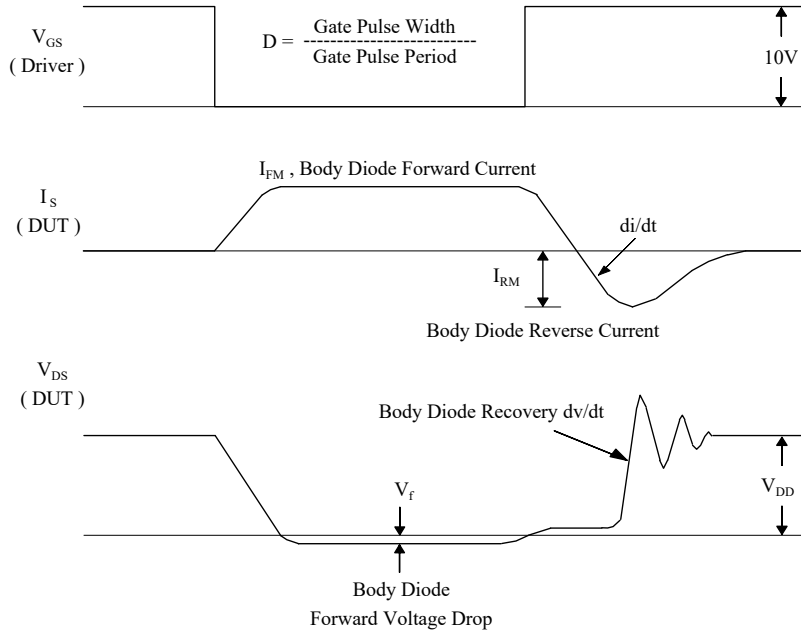
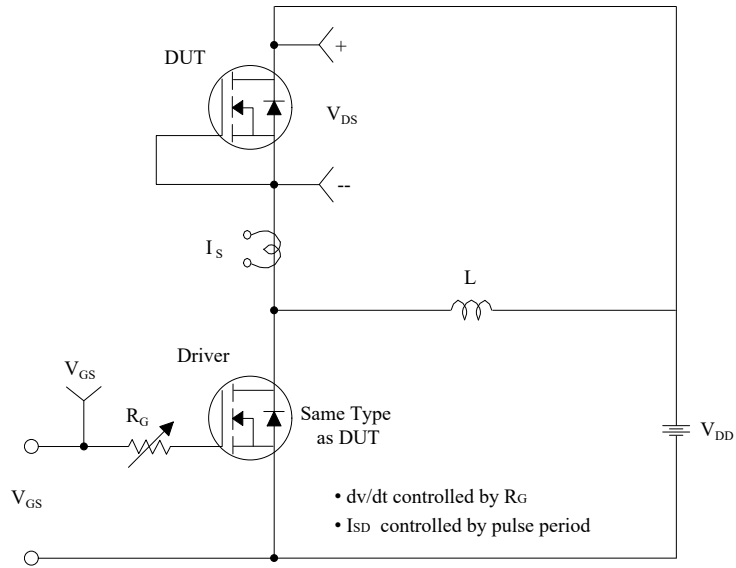


### Unclamped Inductive Switching Test Circuit & Waveforms

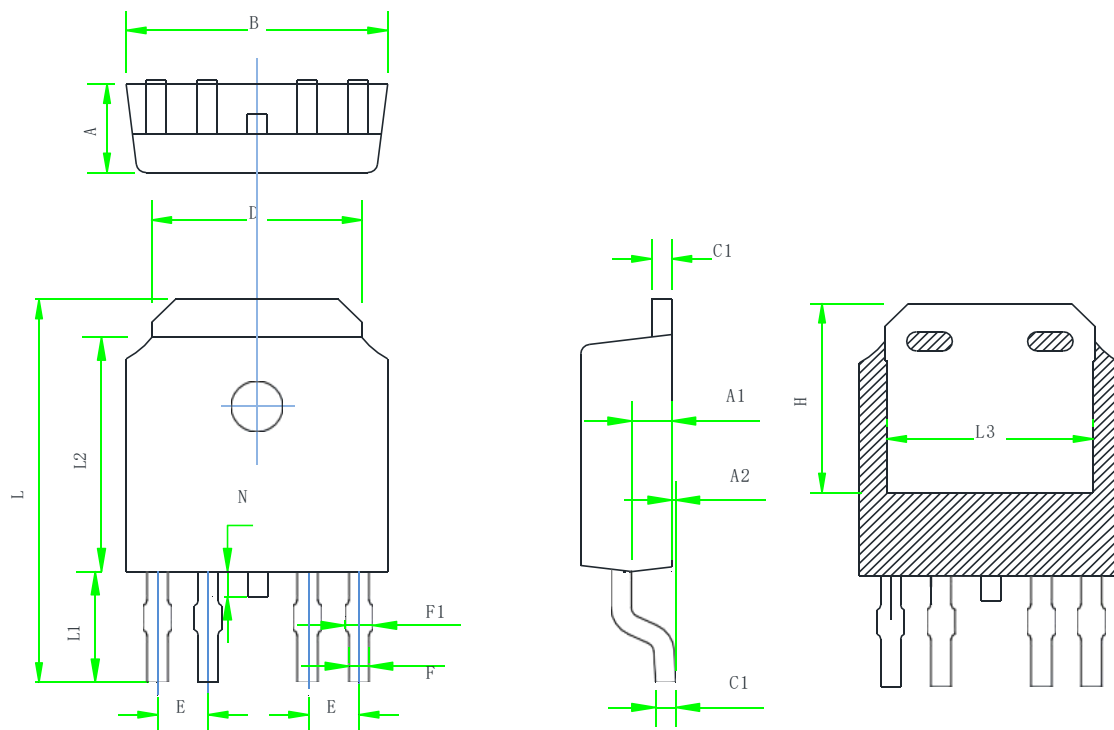




# Peak Diode Recovery dv/dt Test Circuit & Waveforms



## TO-252 -4L OUTLINE



SYMBOL	Mechanical Dimensions/mm			SYMBOL	Mechanical Dimensions/mm		
	MIN	NOM	MAX		MIN	NOM	MAX
A	2.10	2.30	2.45	E	-	1.27type	-
A1	0.85	1.01	1.15	F1	0.40	0.60	0.80
A2	0.05	0.15	0.25	F	0.38	0.50	0.65
B	6.35	6.60	6.80	H	4.55	4.90	5.25
C	0.40	0.50	0.60	L	9.60	10.00	10.30
C1	0.40	0.50	0.60	L1	2.50	2.80	3.10
D	5.05	5.32	5.55	L2	5.85	6.10	6.35
N	0.40	0.65	0.90	L3	4.85	5.20	5.55

## Disclaimer

The content specified herein is for the purpose of introducing Msemitek's products (here in after "Products"). The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Msemitek does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of the Products or technical information described in this document.

The products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). Msemitek shall bear no responsibility in any way for use of any of the Products for the above special purposes.

Although, Msemitek endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Msemitek's product.

The content specified herein is subject to change for improvement without notice. When using a Msemitek's product, be sure to obtain the latest specifications.