

SLP13N50A / SLF13N50A

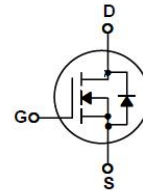
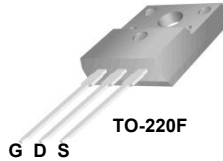
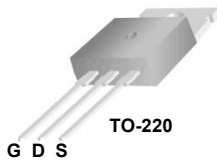
500V N-Channel MOSFET

General Description

This Power MOSFET is produced using Msemitek's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 13A, 500V, $R_{DS(on)} = 0.42\Omega @ V_{GS} = 10V$
- Low gate charge (typical 19.1nC)
- Low C_{rss} (typical 4.6pF)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SLP13N50A	SLF13N50A	Units
V_{DSS}	Drain-Source Voltage	500		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	13		A
	- Continuous ($T_C = 100^\circ\text{C}$)	6.4*		A
I_{DM}	Drain Current - Pulsed (Note 1)	40*		A
V_{GSS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	346		mJ
I_{AR}	Avalanche Current (Note 1)	10		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	41		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	32.5		W
	- Derate above 25°C	0.26		W/ $^\circ\text{C}$
T_j, T_{stg}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	SLP13N50A	SLF13N50A	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	4.0		$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	--		$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	47.8		$^\circ\text{C}/\text{W}$

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLP13N50A	SLP13N50A	T0-220C	Tube	1000	5000
SLF13N50A	SLF13N50A	T0-220F	Tube	1000	5000

Electrical Characteristics TC = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	500			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A, \text{Referenced to } 25^\circ C$		0.51		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500V, V_{GS} = 0V$			1	μA
		$V_{DS} = 400V, T_C = 125^\circ C$			10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics						
$V_{GS(TH)}$	Gate Threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0		4.0	V
$R_{DS(On)}$	Drain-Source on-state resistance	$V_{GS} = 10V, I_D = 5A, T_J = 25^\circ C$		0.42	0.54	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40V, I_D = 5A$ (Note 4)		7.5		S
Dynamic Characteristics						
C_{iss}	Input capacitance	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0 \text{ MHz}$		1066		pF
C_{oss}	Output capacitance			153		pF
C_{riss}	Reverse transfer capacitance			4.6		pF
Switching Characteristics						
$t_{d(on)}$	Turn On Delay Time	$V_{DD} = 250V, I_D = 10A, R_G = 25 \Omega$ (Note 4, 5)		20		ns
t_r	Rising Time			32		ns
$t_{d(off)}$	Turn Off Delay Time			64		ns
t_f	Fall Time			32		ns
Q_g	Total Gate Charge	$V_{DS} = 400V, I_D = 10A, V_{GS} = 10V$ (Note 4, 5)		19.1		nC
Q_{gs}	Gate-Source Charge			5.5		nC
Q_{gd}	Gate-Drain Charge			6.4		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				10	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				40	A
V_{SD}	Diode Forward Voltage	$V_{GS} = 0V, I_S = 10A$			1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V, I_S = 10A, di_F / dt = 100 \text{ A}/\mu s$ Note 4)		320		ns
Q_{rr}	Reverse Recovery Charge			2.2		μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 7.2 \text{ mH}, V_{DD} = 50V, R_G = 25 \Omega, \text{Starting } T_J = 25^\circ C$
3. $I_{SD} \leq 10A, di/dt \leq 200A/\mu s, V_{DD} \leq BVDSS, \text{Starting } T_J = 25^\circ C$
4. Pulse Test : Pulse width $\leq 300\mu s, \text{Duty cycle } \leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

Table 7 Reverse diode characteristics

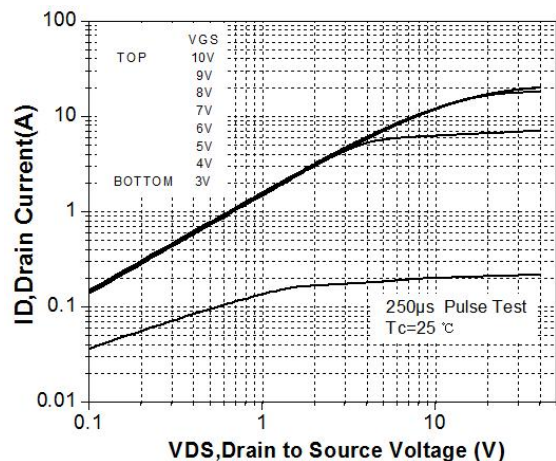


Figure 1. On-Region Characteristics

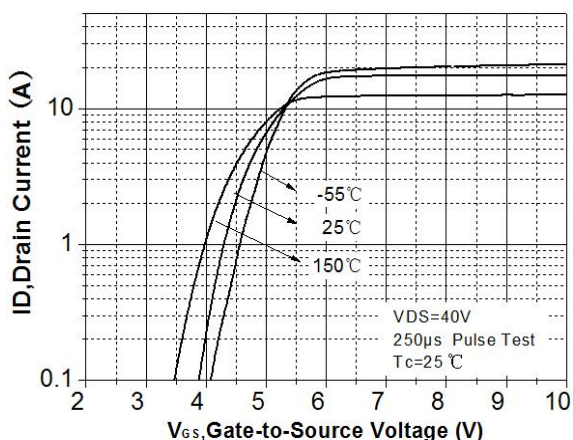


Figure 2. Transfer Characteristics

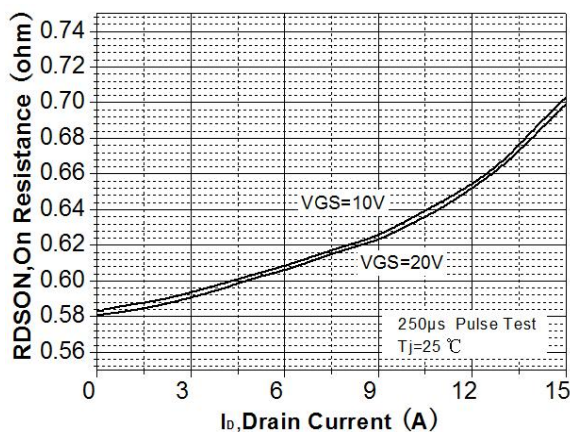


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

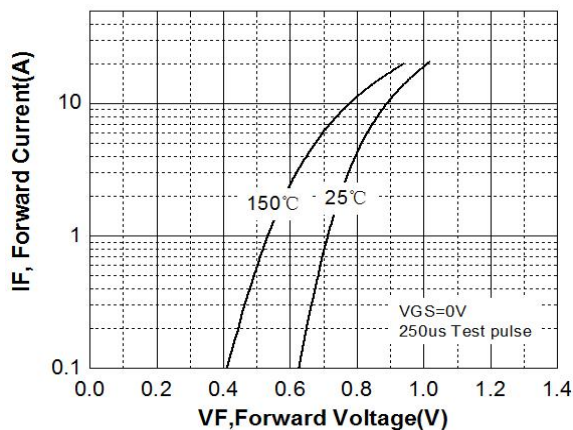


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

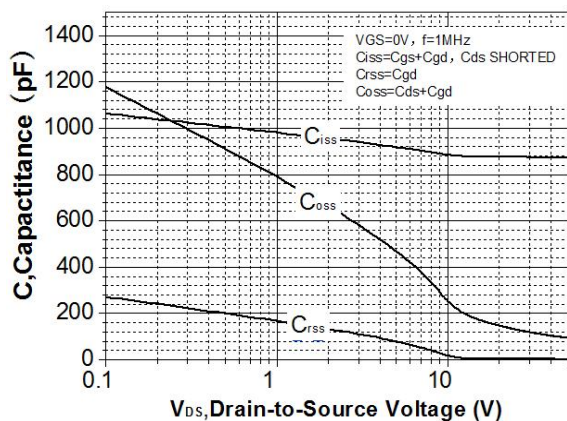


Figure 5. Capacitance Characteristics

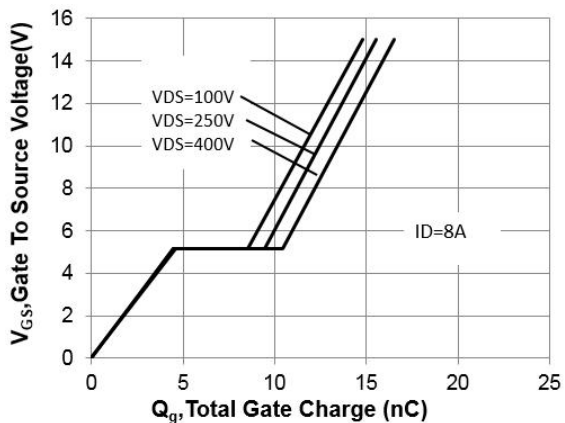


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

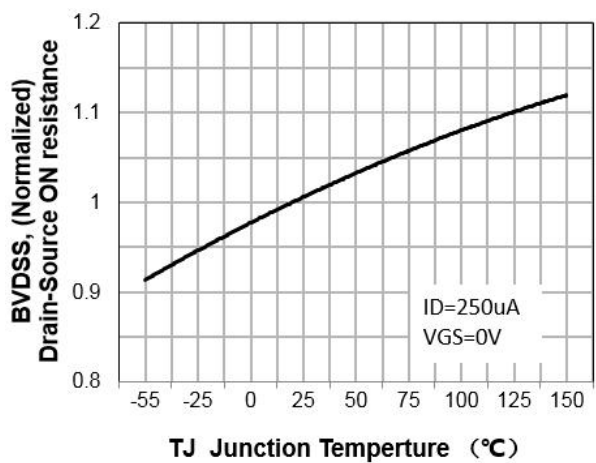


Figure 7. Breakdown Voltage Variation vs Temperature

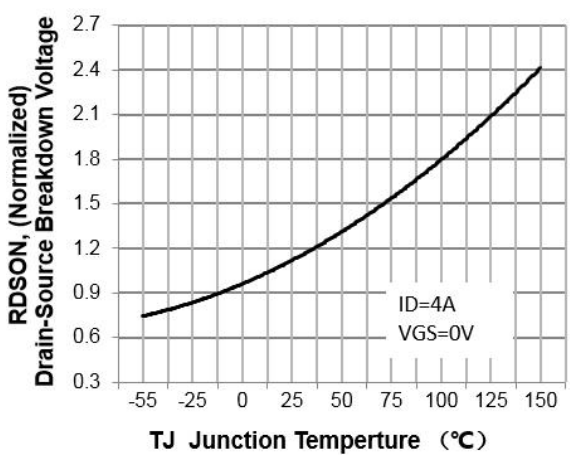


Figure 8. On-Resistance Variation vs Temperature

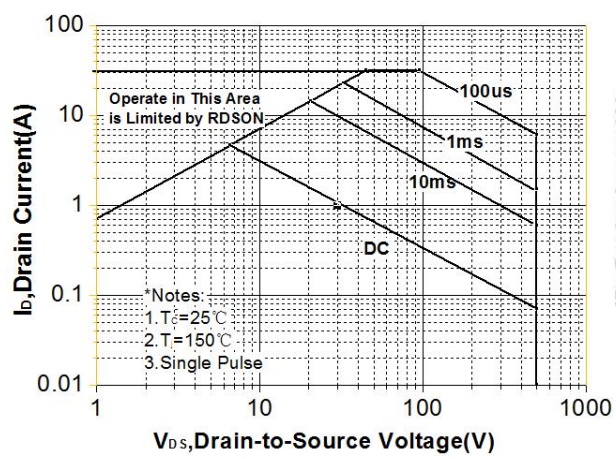


Figure 9. Maximum Safe Operating Area

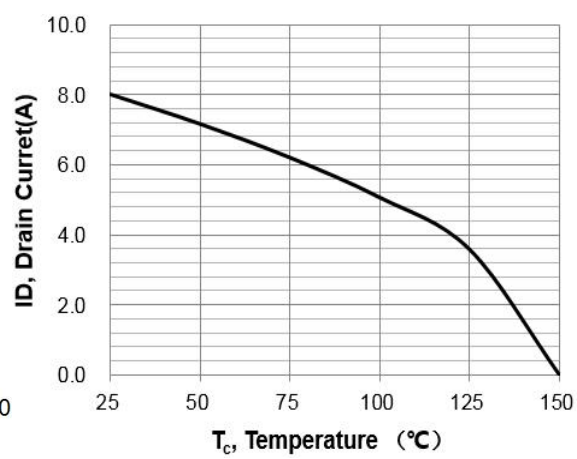


Figure 10. Maximum Drain Current vs Case Temperature

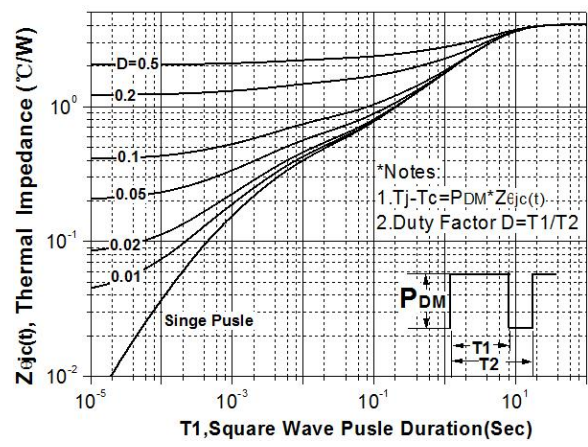
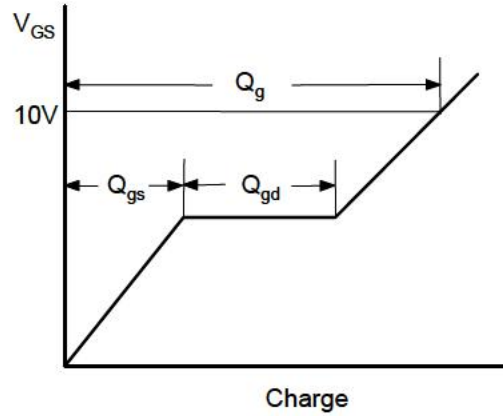
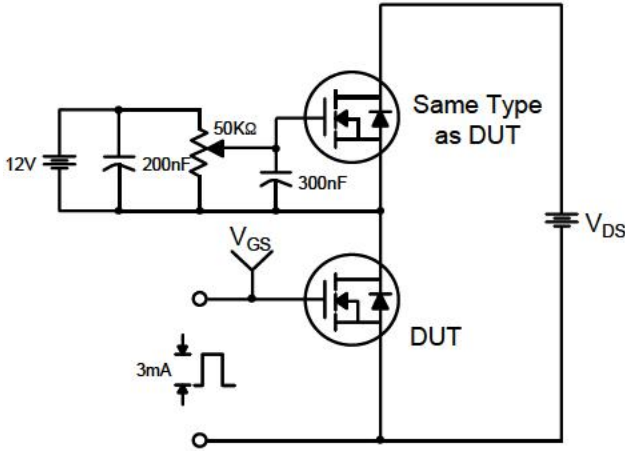
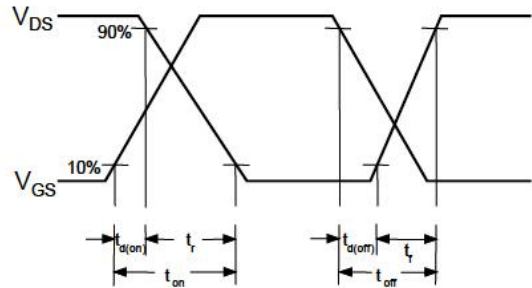
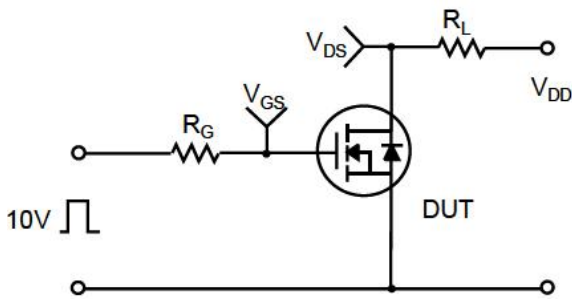


Figure 11. Transient Thermal Response Curve

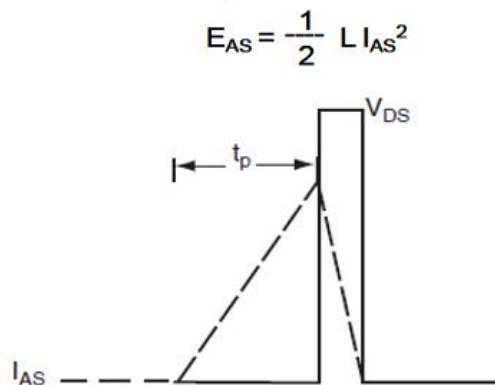
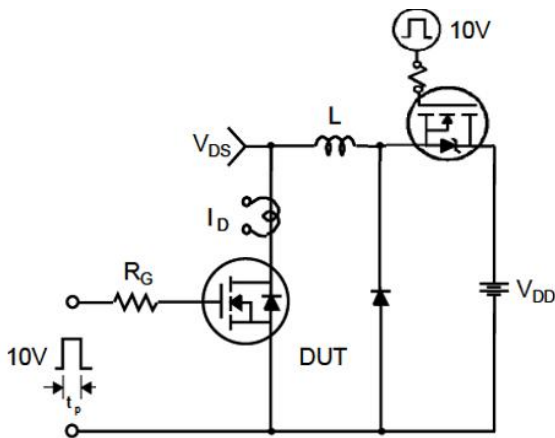
Gate Charge Test Circuit & Waveform



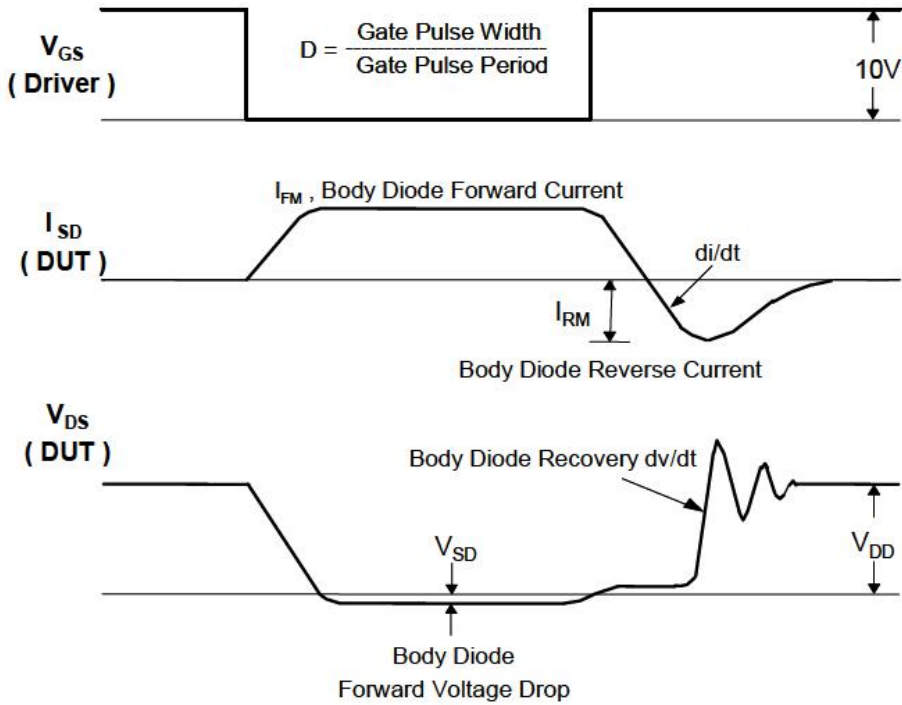
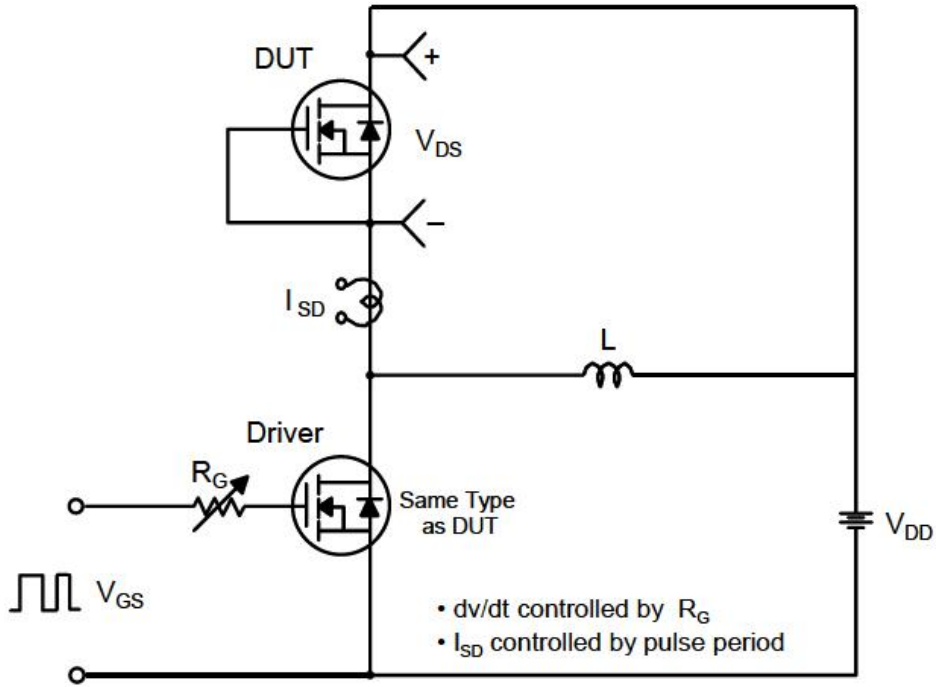
Resistive Switching Test Circuit & Waveforms



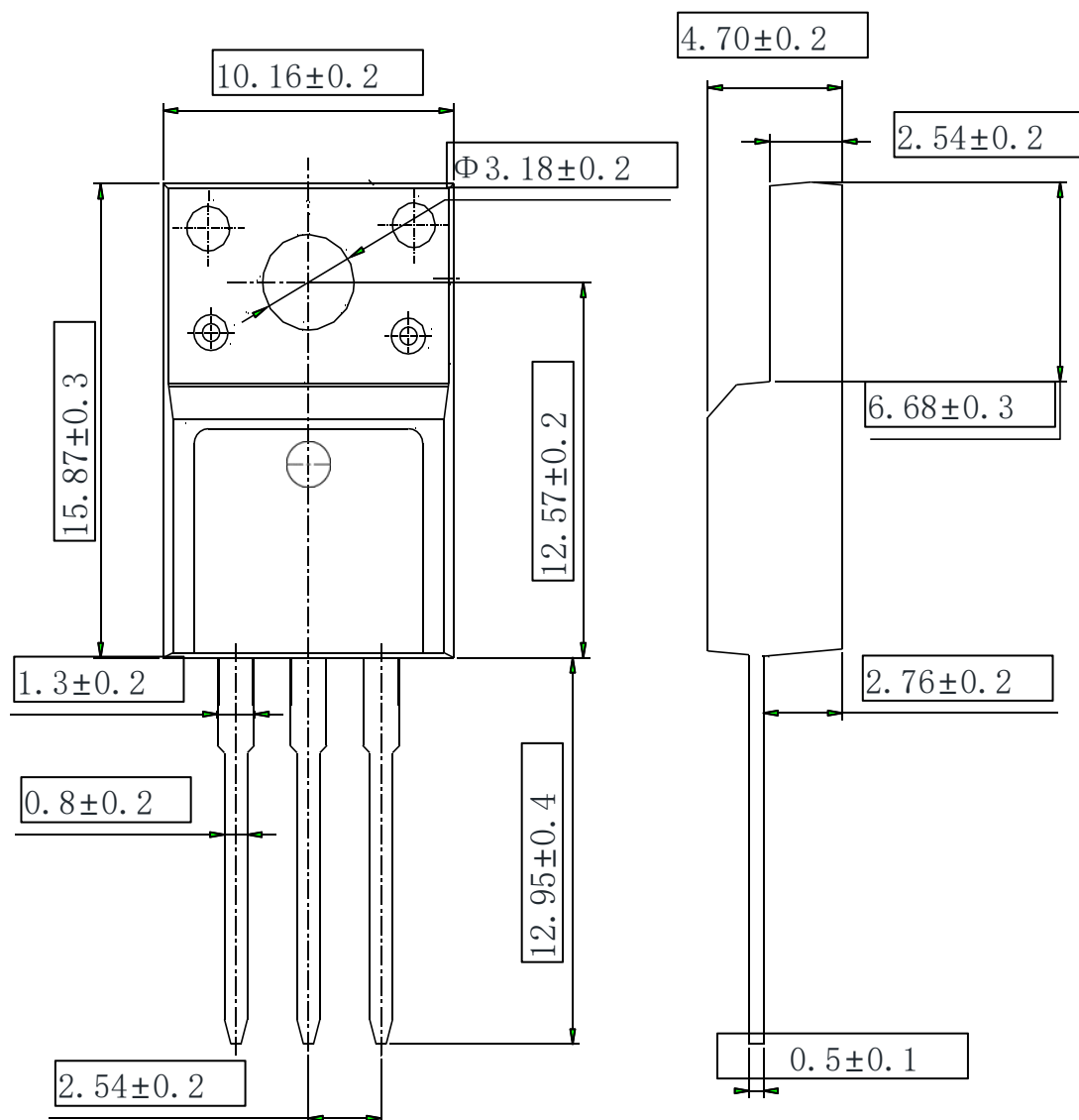
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



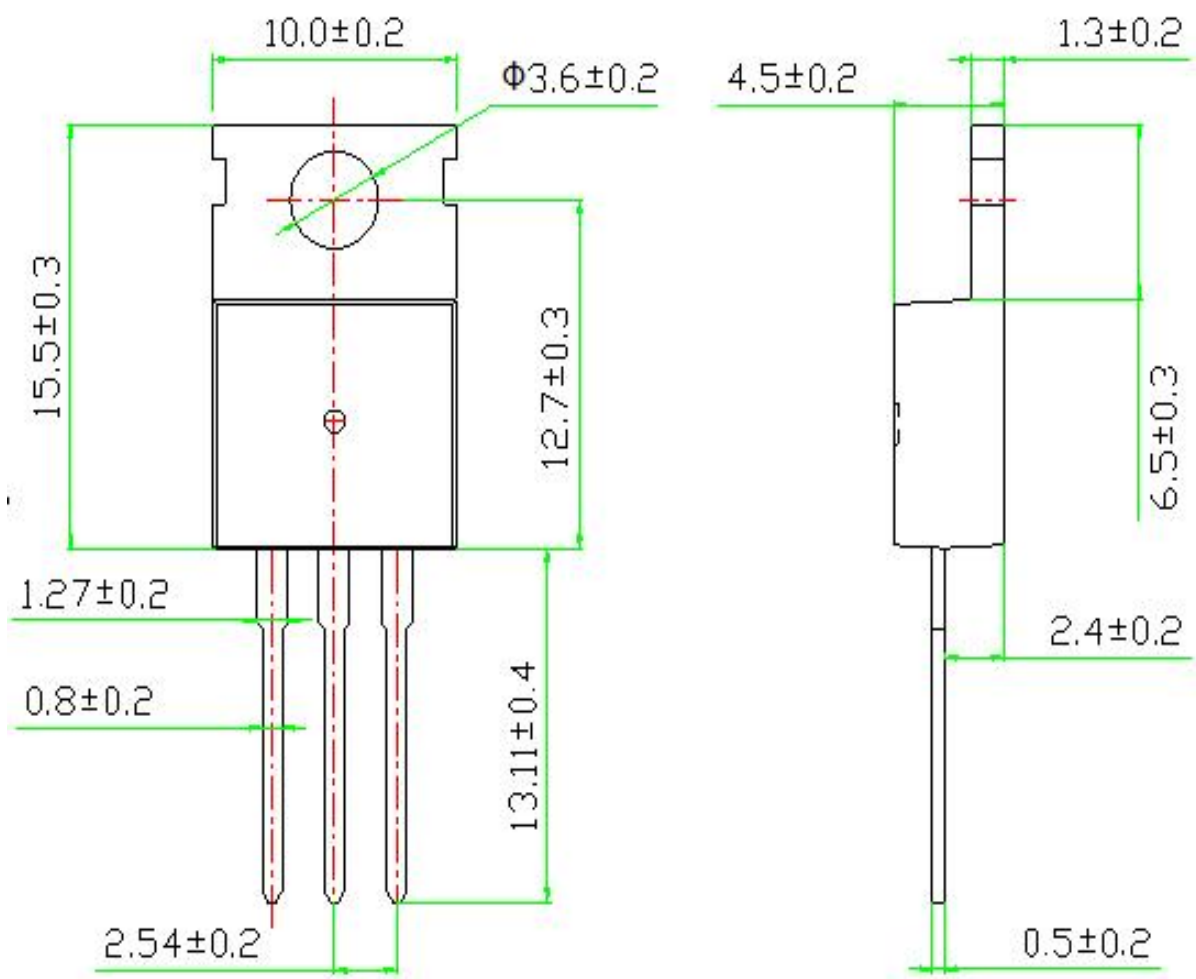
TO-220F OUTLINE



NOTE :

- 1The plastic package is not marked as smooth surface $Ra=0.1$; Subglossy surface $Ra=0.8$
2. Undeclared tolerance ± 0.15 , Unmarked fillet $R_{max}=0.25$

TO-220C OUTLINE



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