

# SLD05P06T

## 60V P -Channel MOSFET

### General Description

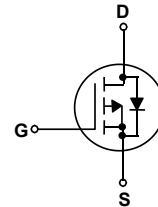
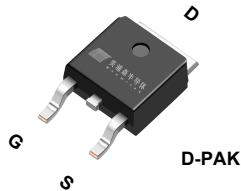
This Power MOSFET is produced using Msemitek's advanced TRENCH technology. This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

### Application

- PWM Application
- Load Switch
- Power Management

### Features

- P-Channel: -60V -5A
- $R_{DS(on)Typ} = 82m\Omega @ V_{GS} = -10V$
- $R_{DS(on)Typ} = 90m\Omega @ V_{GS} = -4.5V$
- Very Low On-resistance  $R_{DS(ON)}$
- Low  $C_{rss}$
- Fast switching
- 100% avalanche tested
- Improved  $dv/dt$  capability



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	SLD05P06T	Units
$V_{DSS}$	Drain-Source Voltage	-60	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ ) - Continuous ( $T_C = 100^\circ C$ )	-5	A
		-3.2	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	-20	A
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	49	mJ
$P_D$	Power Dissipation ( $T_C = 25^\circ C$ )	74	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.7	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ C$

\* Drain current limited by maximum junction temperature.

## Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLD05P06T	SLD05P06T	TO-252	Tape & Reel	2500	25000

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-60	--	--	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.0	-1.7	-2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -4\text{ A}$	--	82	100	m $\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -2\text{ A}$	--	90	110	

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	946	-	pF
$C_{oss}$	Output Capacitance		--	50	-	pF
$C_{riss}$	Reverse Transfer Capacitance		--	41	-	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V},$ (Note 3) $R_G = 3.3\text{ }\Omega, I_D = -4\text{ A}, T_J = 25^\circ\text{C}$	--	6.5	--	ns
$t_r$	Turn-On Rise Time		--	22	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	41	--	ns
$t_f$	Turn-Off Fall Time		--	10	--	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -4\text{ A},$ $V_{GS} = -10\text{ V}$ (Note 3)	--	30	--	nC
$Q_{gs}$	Gate-Source Charge		--	4.5	--	nC
$Q_{gd}$	Gate-Drain Charge		--	4.7	--	nC
$R_G$	Gate Resistance	$f = 1\text{ MHz}$	--	11	--	$\Omega$

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	-5	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-20	A
$V_{SD}$	Drain to Source Diode Forward Voltage, $V_{GS} = 0\text{ V}, I_{SD} = -10\text{ A}, T_J = 25^\circ\text{C}$	--	--	-1.2	V

#### Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition:  $T_J = 25^\circ\text{C}, V_{DD} = -40\text{ V}, V_G = -10\text{ V}, L = 0.5\text{ mH}$ .
3. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$

### P- Channel Typical Characteristics

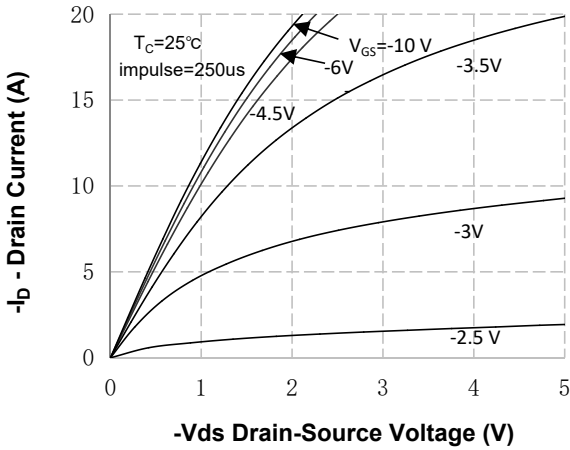


Figure 1. On-Region Characteristics

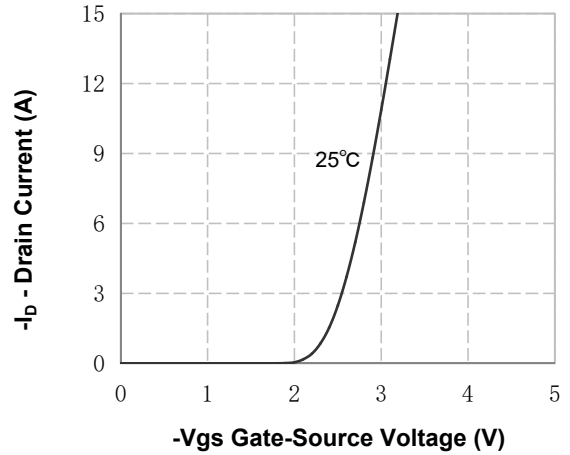


Figure 2. Transfer Characteristics

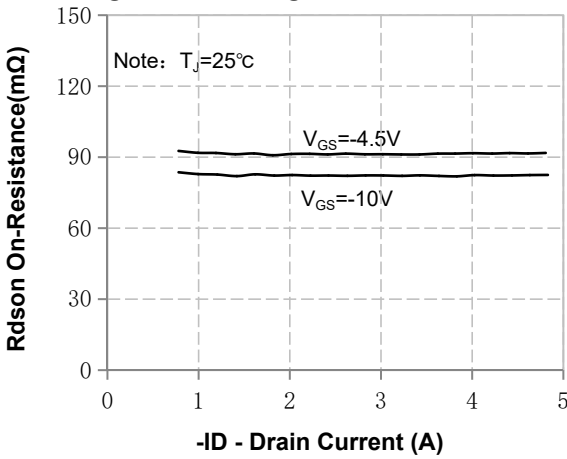


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

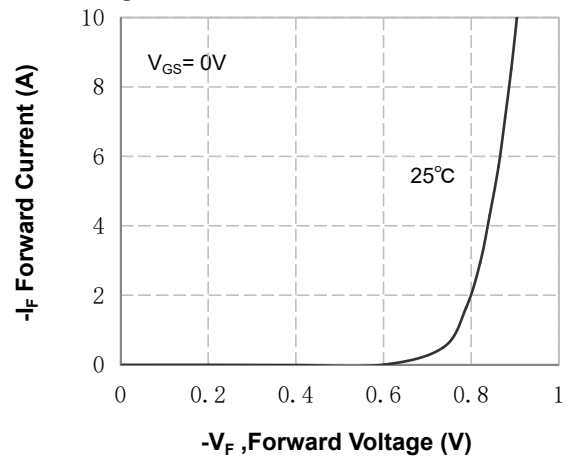


Figure 4. Body Diode Forward Voltage Variation with Source Current

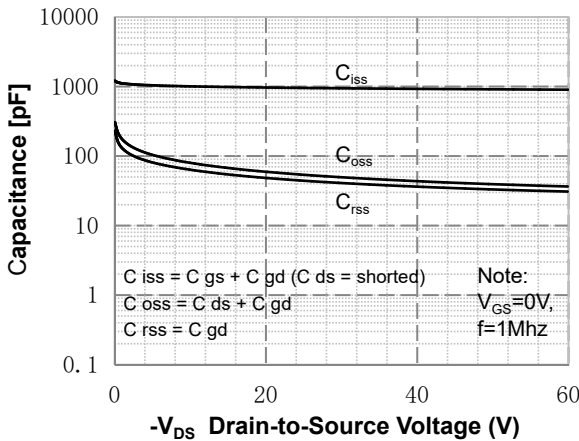


Figure 5. Capacitance Characteristics

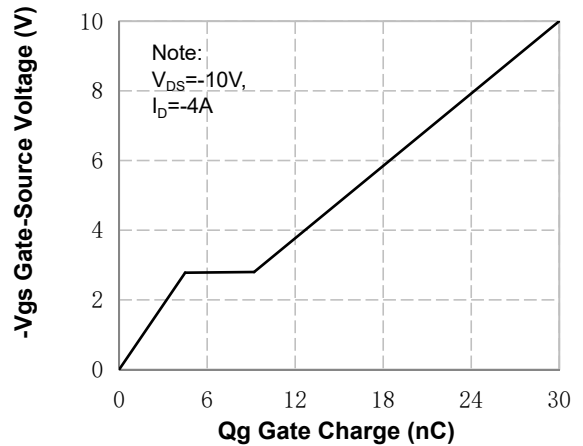
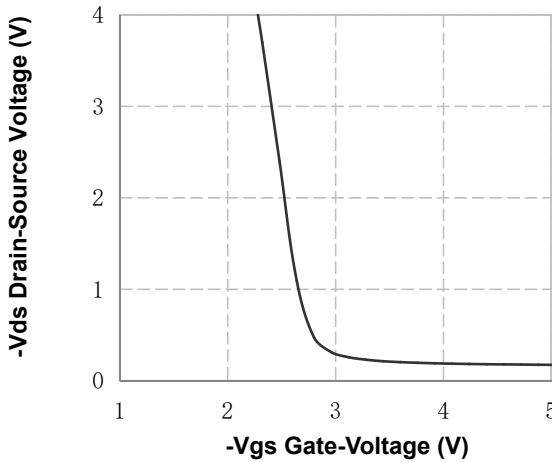
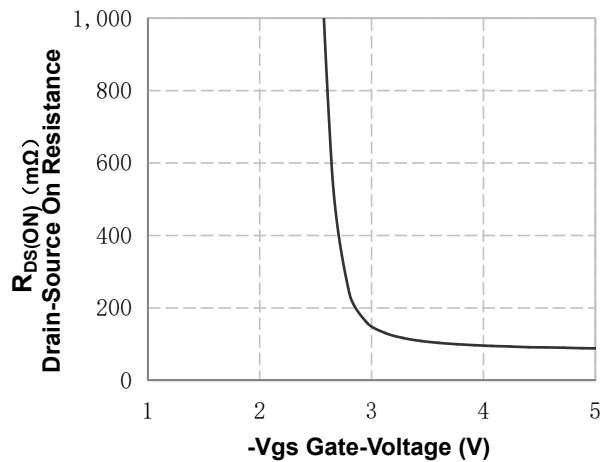


Figure 6. Gate Charge Characteristics

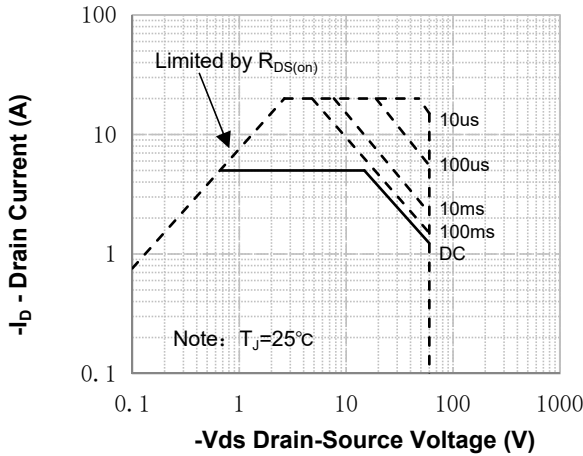
**P- Channel Typical Characteristics** (Continued)



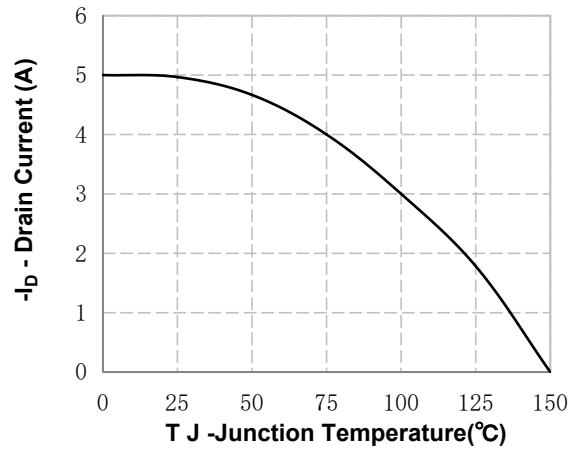
**Figure 7. Vds Drain-Source Voltage vs Gate Voltage**



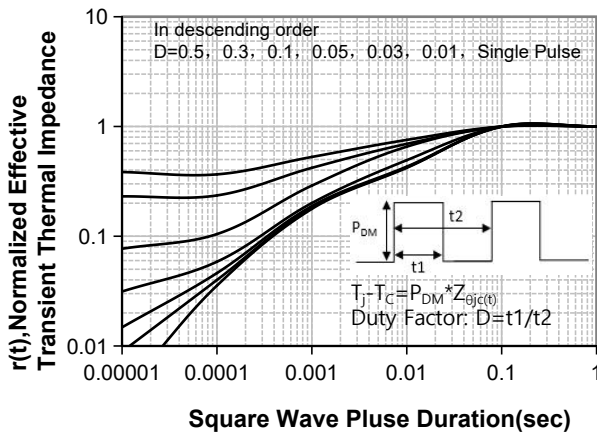
**Figure 8. On-Resistance vs Gate Voltage**



**Figure 9. Maximum Safe Operating Area**



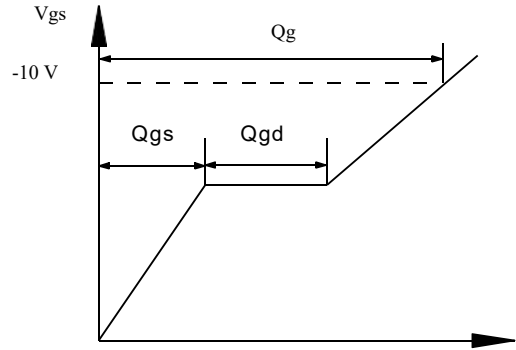
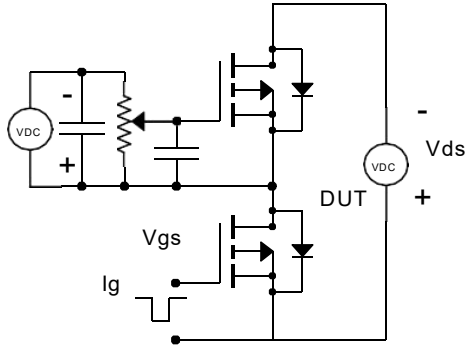
**Figure 10. Maximum Continuous Drain Current vs Temperature**



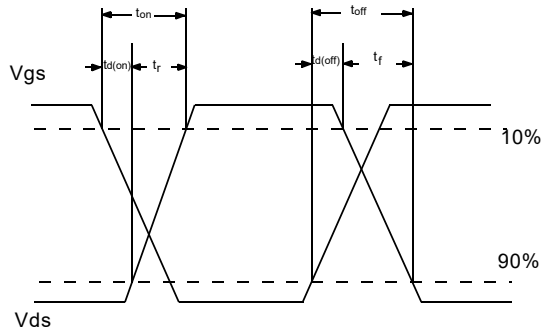
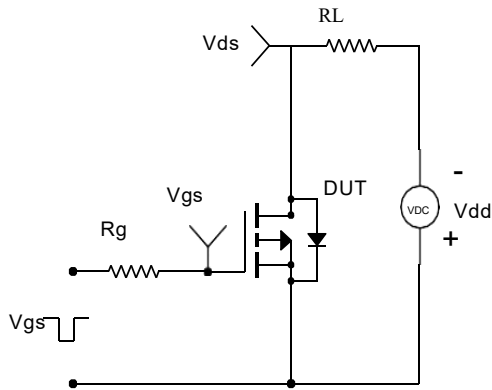
**Figure 11. Transient Thermal Response Curve**

**P- Channel**

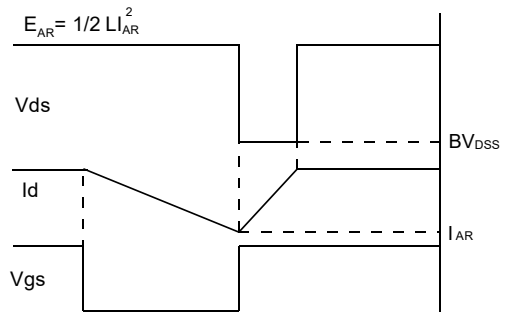
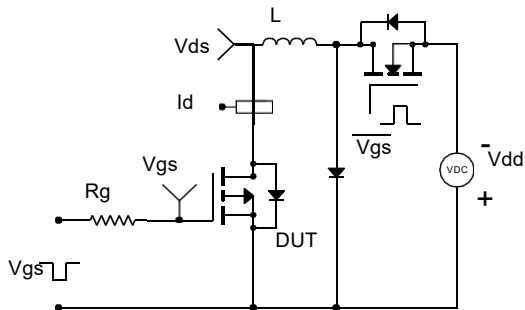
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**

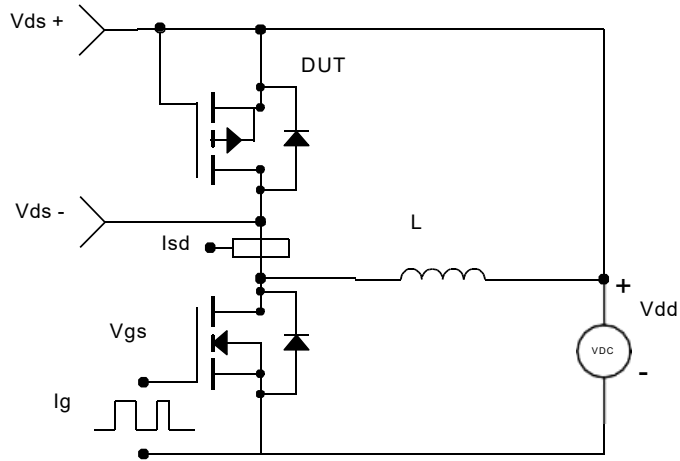


**Unclamped Inductive Switching Test Circuit & Waveforms**

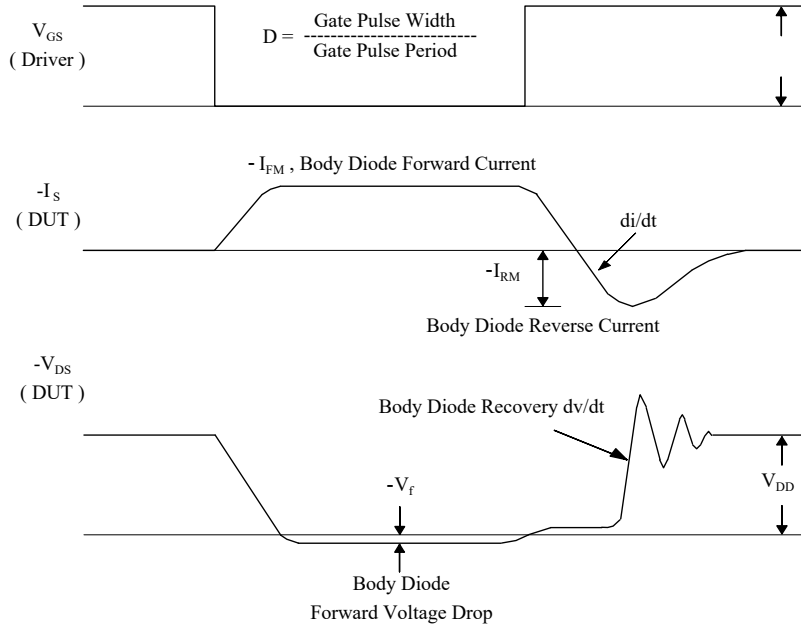


P- Channel

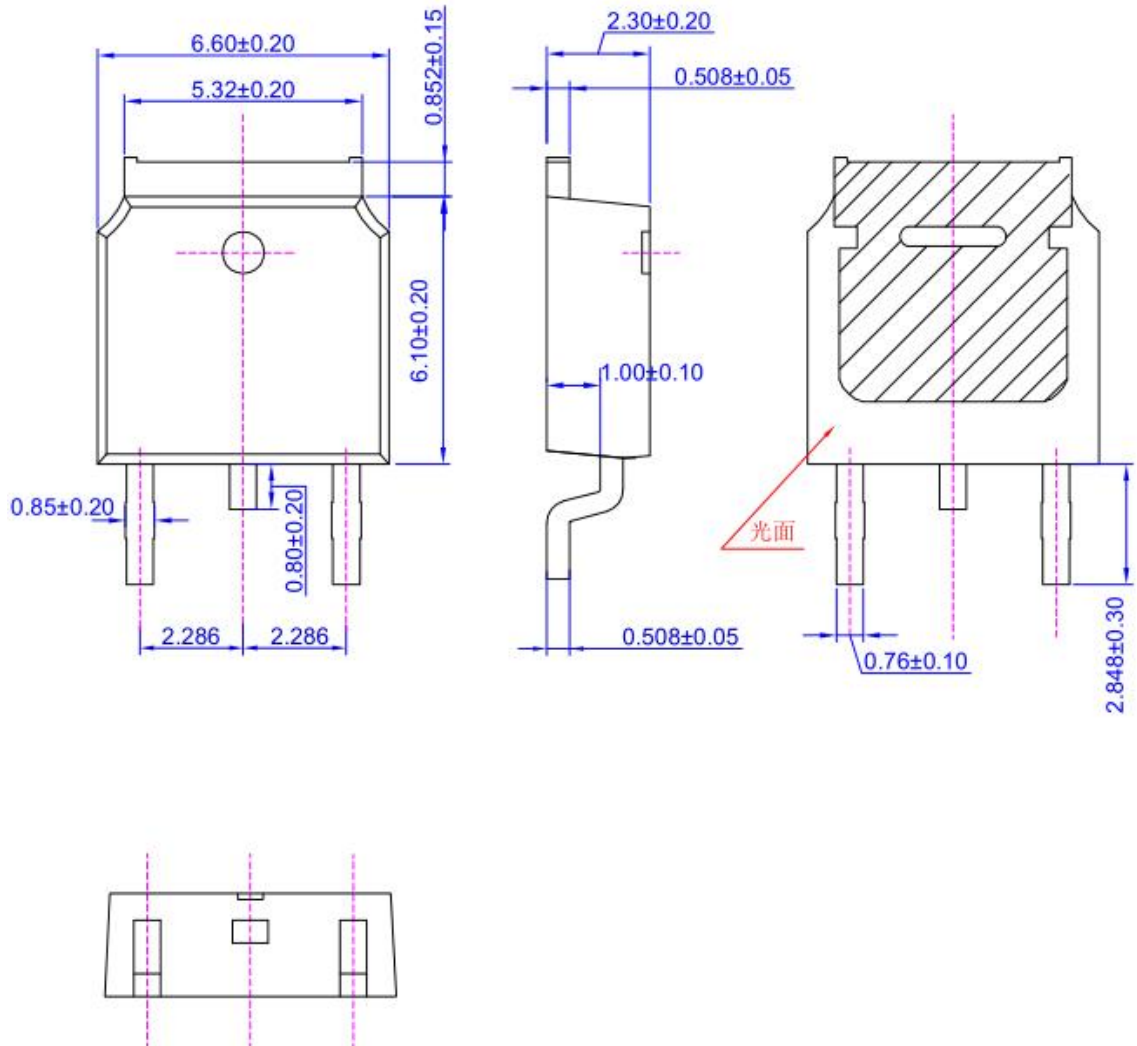
Peak Diode Recovery dv/dt Test Circuit & Waveforms



- $dv/dt$  controlled by  $R_G$
- $I_{SD}$  controlled by pulse period



## TO-252 OUTLINE



## NOTE:

- 1The plastic package is not marked as smooth surface  $Ra=0.1$ ; Subglossy surface  $Ra=0.8$
2. Undeclared tolerance  $\pm 0.25$ , Unmarked fillet  $R_{max}=0.25$

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