

SLU9N20T/SLD9N20T

200V N-Channel MOSFET

General Description

This Power MOSFET is produced using Msemitek's advanced TRENCH technology.

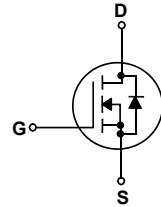
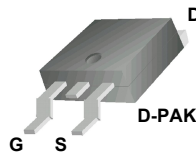
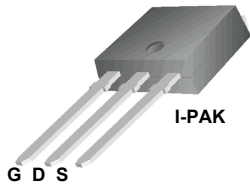
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Application

- PWM Application
- Load Switch
- Power Management

Features

- N-Channel: 200V 9A
 $R_{DS(on)Typ} = 220m\Omega @ V_{GS} = 10V$
- Very Low On-resistance $R_{DS(on)}$
- Low C_{rss}
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	SLU9N20T/SLD9N20T	Units
V_{DSS}	Drain-Source Voltage	200	V
I_D	Drain Current - Continuous ($T_C = 25^\circ C$) - Continuous ($T_C = 100^\circ C$)	9	A
		6	A
I_{DM}	Drain Current - Pulsed (Note 1)	36	A
V_{GSS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy	200	mJ
P_D	Power Dissipation ($T_C = 25^\circ C$)	75	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.67	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to ambient	100	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ C$

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLU9N20T	SLU9N20T	T0-251	Tube	3750	18750
SLD9N20T	SLD9N20T	TO-252	Tape	2500	25000

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	200	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	--	--	1.0	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	-	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$	--	220	330	m Ω

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	494	-	pF
C_{oss}	Output Capacitance		--	92	-	pF
C_{riss}	Reverse Transfer Capacitance		--	50	-	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 100\text{ V},$ $R_L = 25\ \Omega, I_b = 9\text{ A}, T_J = 25^\circ\text{C}$	--	32.5	--	ns
t_r	Turn-On Rise Time		--	7.5	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	19.5	--	ns
t_f	Turn-Off Fall Time		--	4.5	--	ns
Q_g	Total Gate Charge	$V_{DS} = 100\text{ V}, I_D = 9\text{ A},$ $V_{GS} = 10\text{ V}$	--	38	--	nC
Q_{gs}	Gate-Source Charge		--	2.0	--	nC
Q_{gd}	Gate-Drain Charge		--	18.5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	9	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	36	A
V_{SD}	Drain to Source Diode Forward Voltage, $V_{GS} = 0\text{ V}, I_{SD} = 20\text{ A}, T_J = 25^\circ\text{C}$	--	-	1.4	V
T_{rr}	Reverse recovery time, $I_F = 9\text{ A}, D_{IF}/dt = 100\text{ A}/\mu\text{s}$			110	ns
Q_{rr}	Reverse recovery charge, $I_F = 9\text{ A}, D_{IF}/dt = 100\text{ A}/\mu\text{s}$			0.5	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: $T_J = 25^\circ\text{C}, V_{DD} = 30\text{ V}, V_G = 10\text{ V}, L = 10\text{ mH},$
3. Pulse Test: Pulse Widths $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 0.5\%$

N- Channel Typical Characteristics

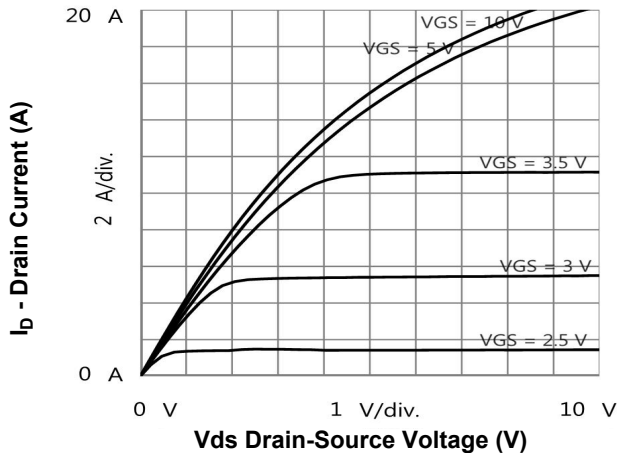


Figure 1. On-Region Characteristics

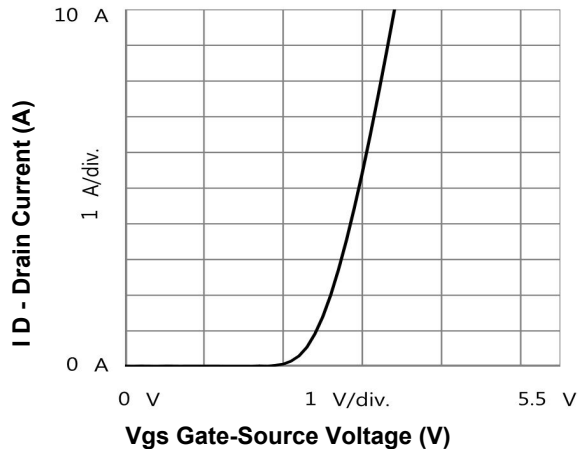


Figure 2. Transfer Characteristics

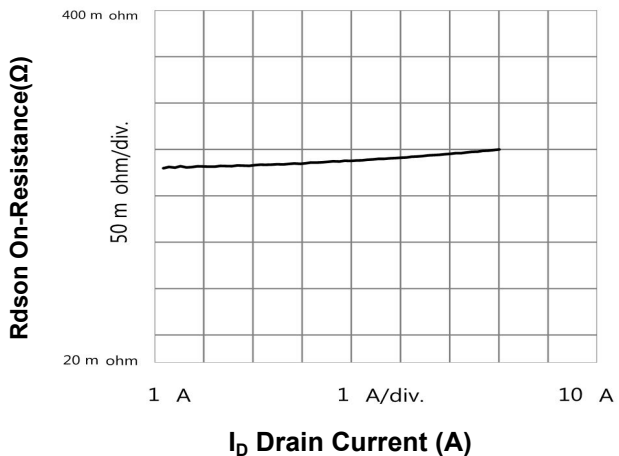


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

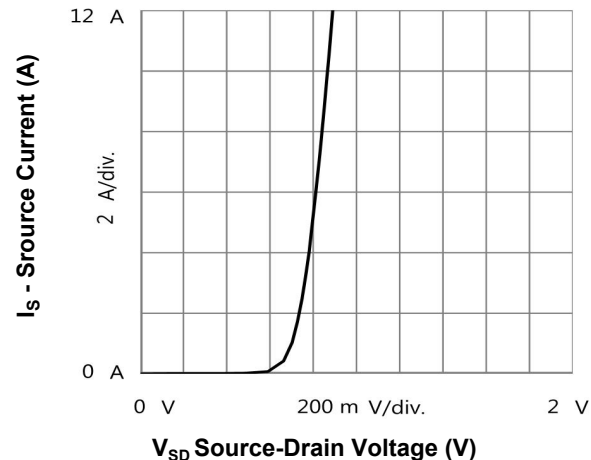


Figure 4. Source Current vs Source-Drain Voltage

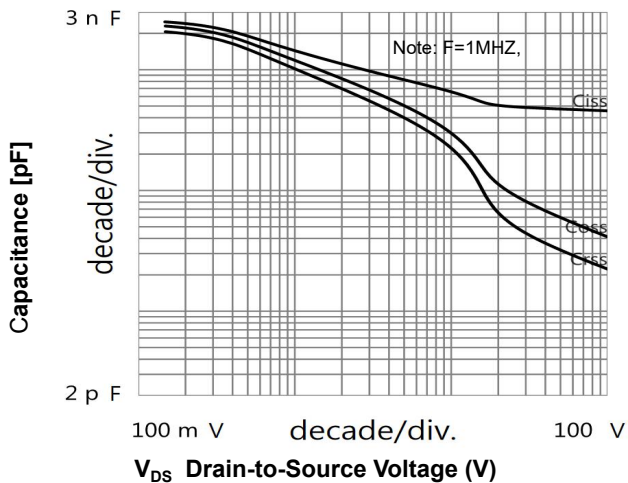


Figure 5.1 Capacitance Characteristics

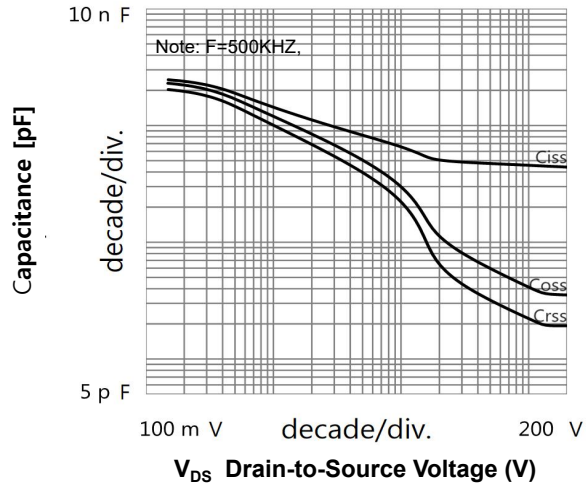


Figure 5.2 Capacitance Characteristics

N- Channel Typical Characteristics (Continued)

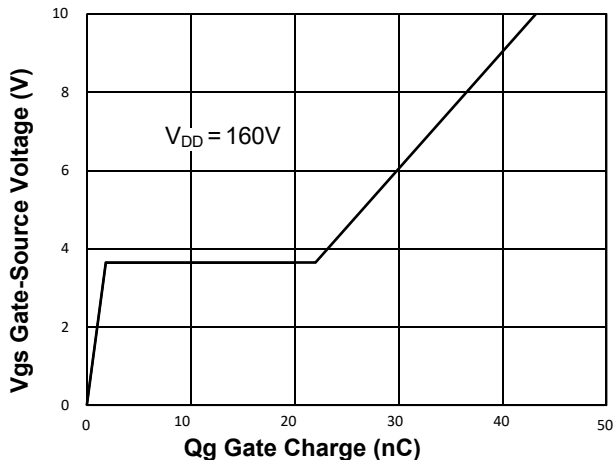


Figure 6. Gate Charge Characteristics

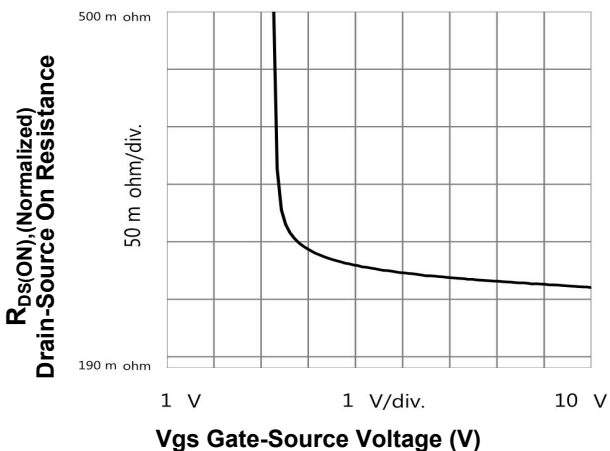


Figure 7. On-Resistance Variation vs Gate-Source Voltage

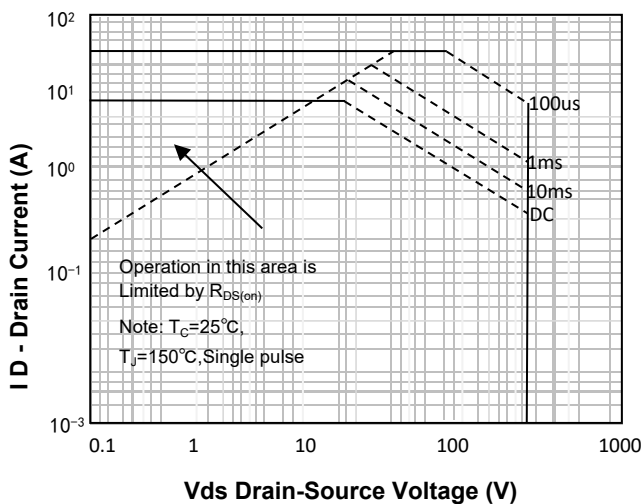


Figure 8. Maximum Safe Operating Area

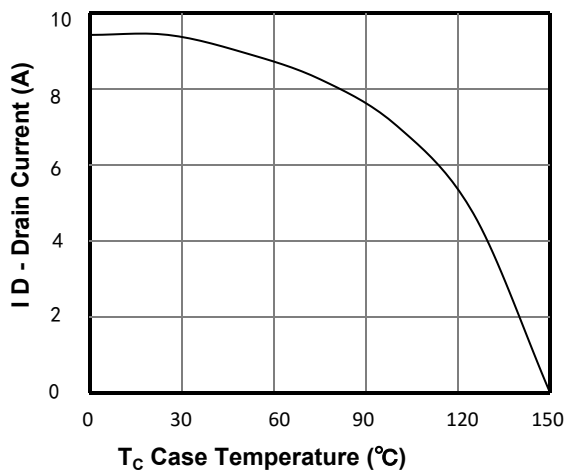


Figure 9. Maximum Drain Current vs Case Temperature

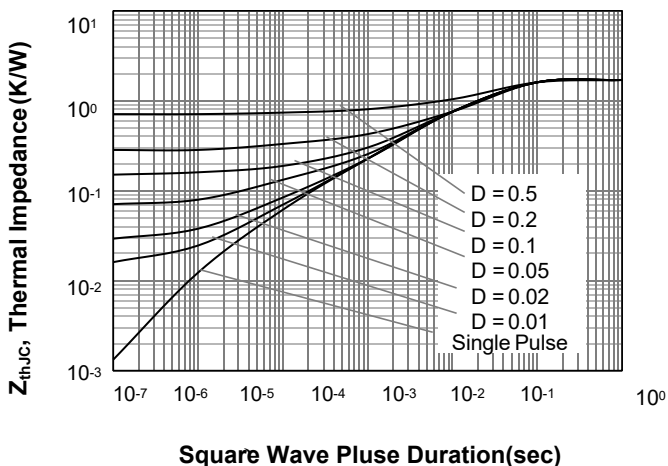
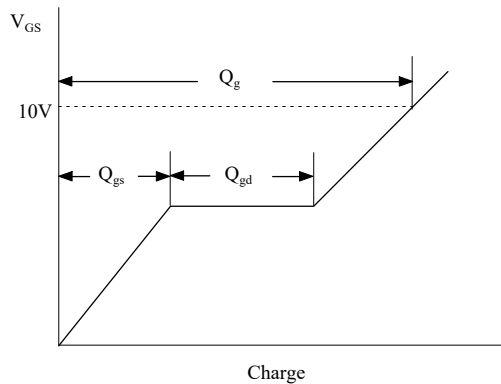
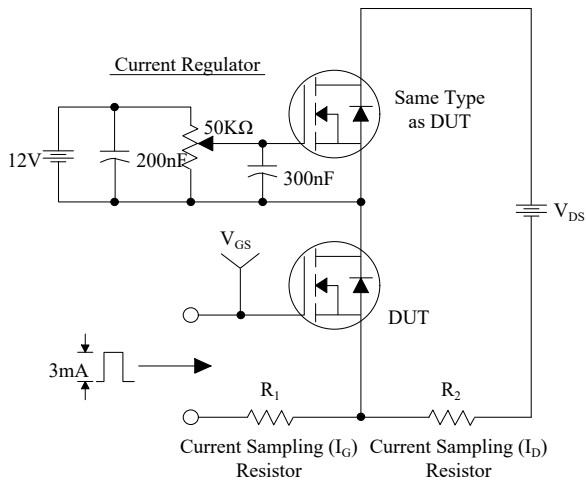
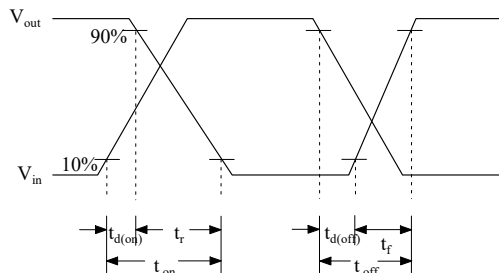
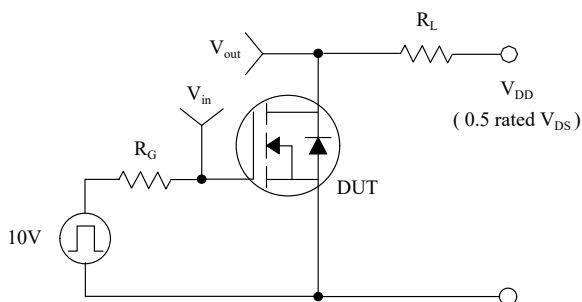


Figure 10. Transient Thermal Response Curve

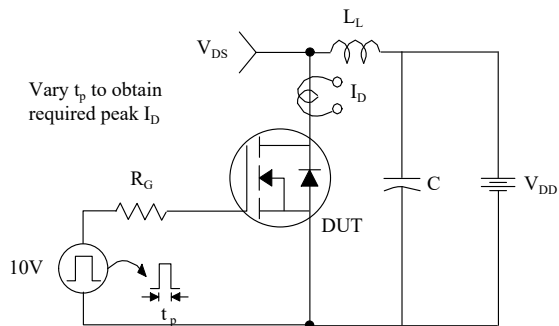
Gate Charge Test Circuit & Waveform



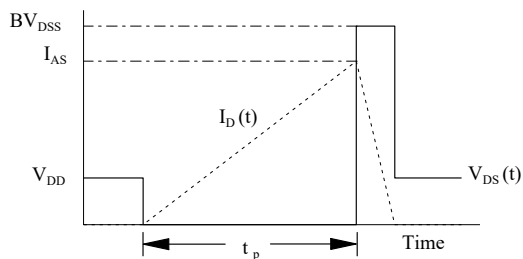
Resistive Switching Test Circuit & Waveforms



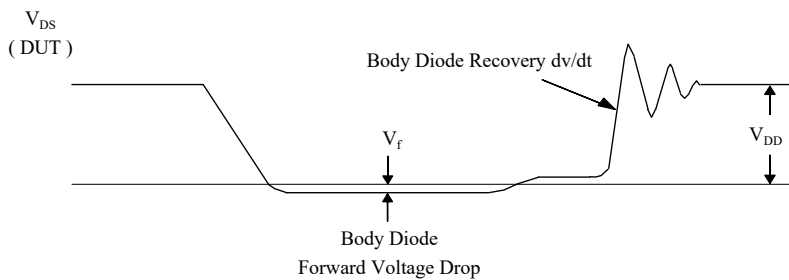
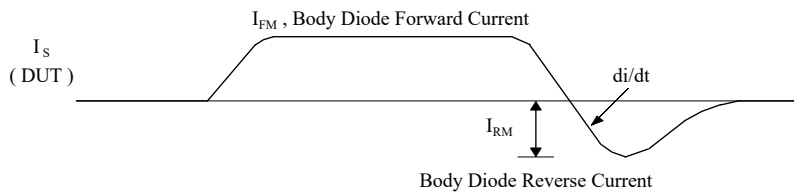
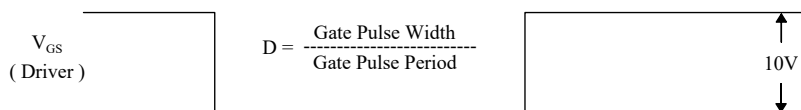
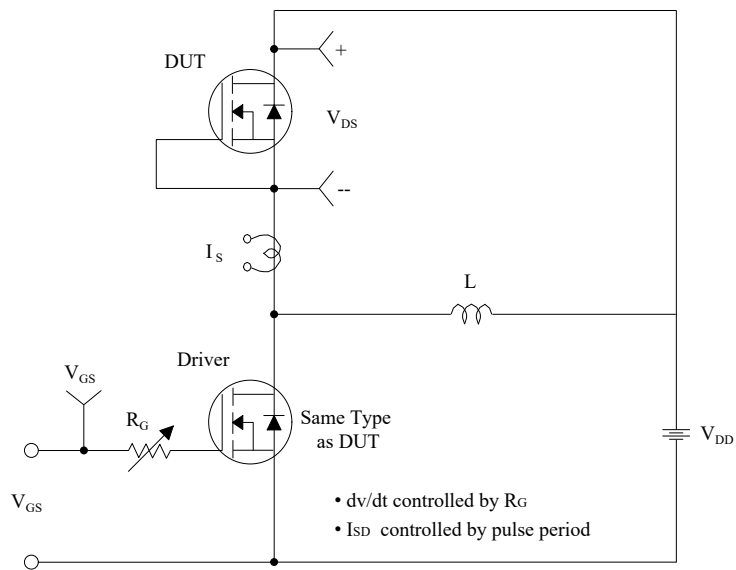
Unclamped Inductive Switching Test Circuit & Waveforms



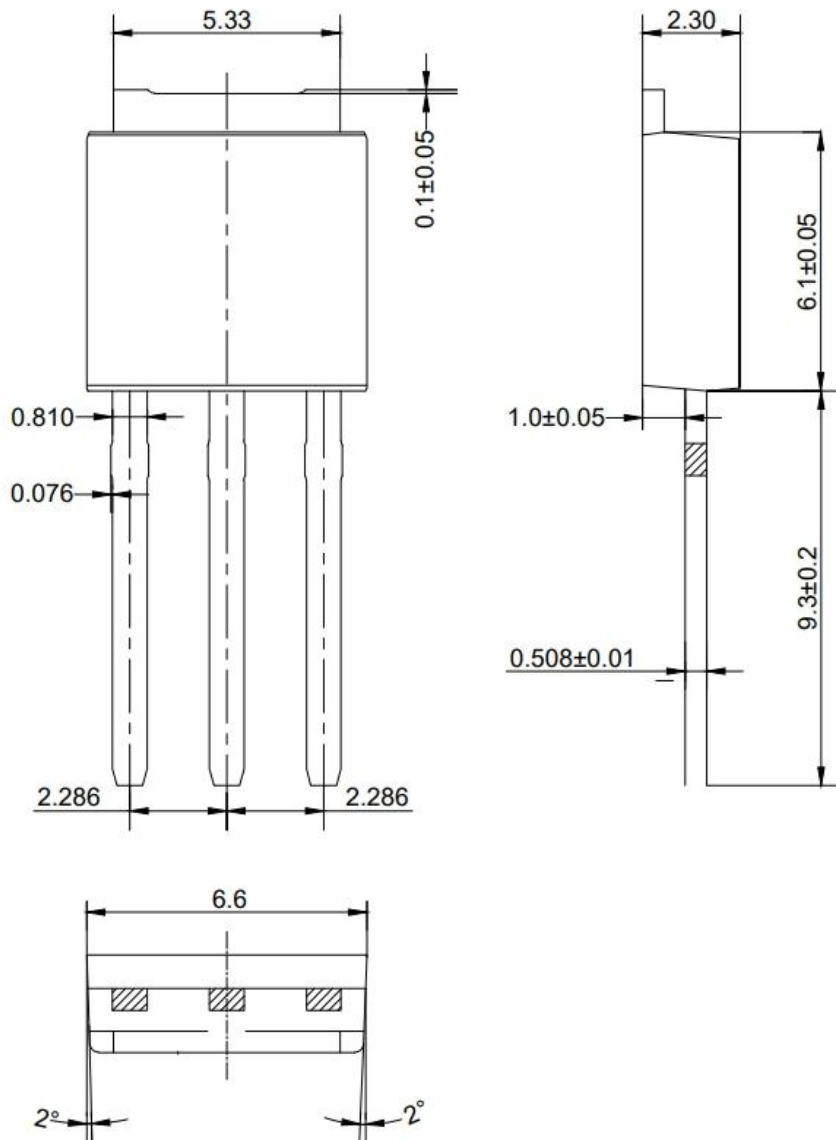
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms



TO-251 OUTLINE

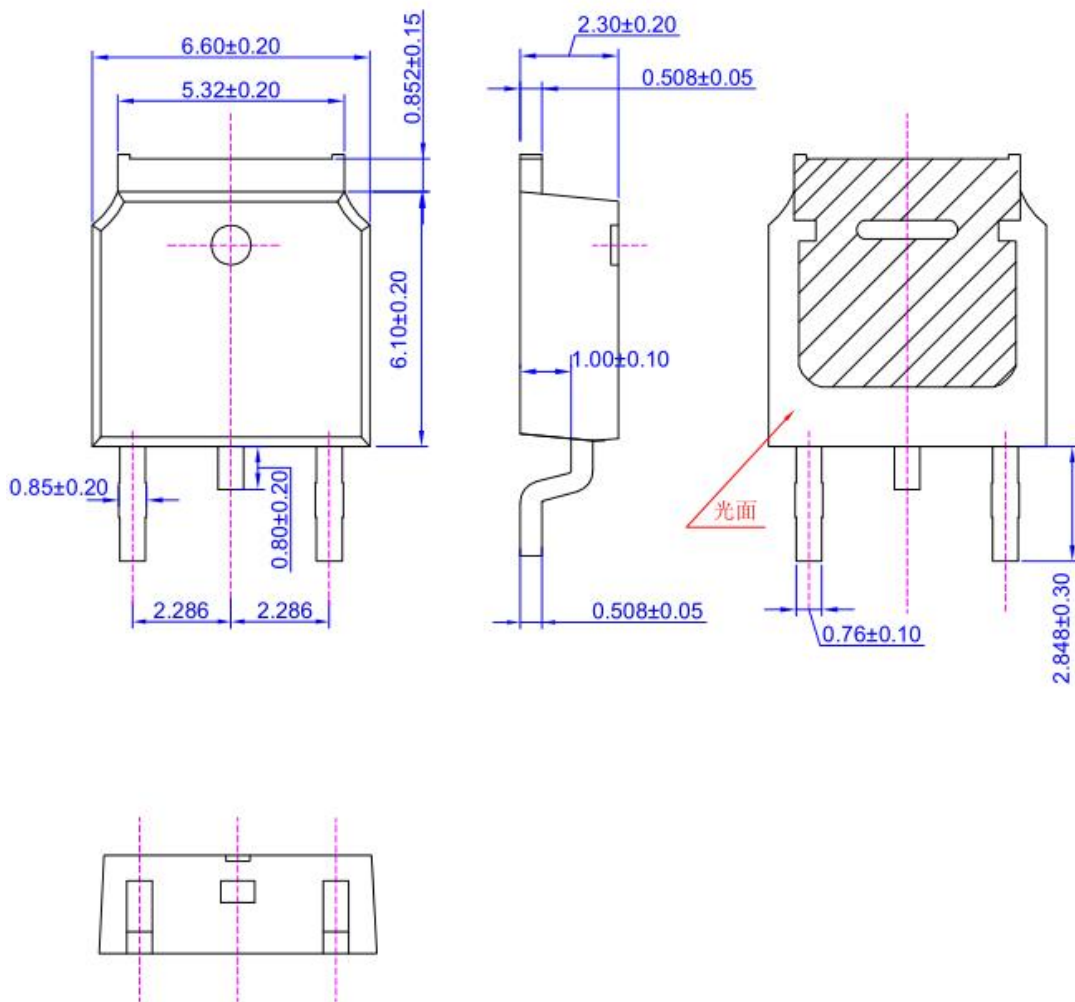


Note:

1,Unit: millimeters

2,The tolerance not noted is ± 0.15 , and the unmarked fillet $R_{max} = 0.25$

TO-252 OUTLINE



NOTE:

- 1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
- 2.Undeclared tolerance ± 0.25 ,Unmarked filletRmax=0.25

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