美浦森半导体
M s e m i t e k

RoHS
LEAD FREE

SLM30L03T
N And P-Channel Enhancement Mode MOSFET

General Description

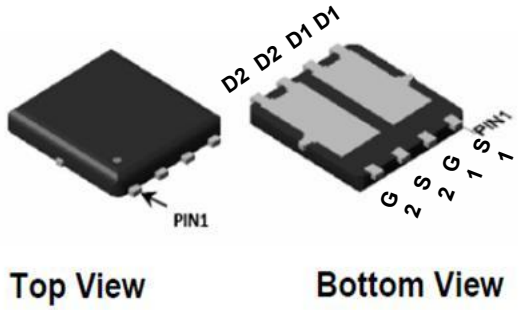
This Power MOSFET is produced using Msemitek's advanced TRENCH technology.
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Features

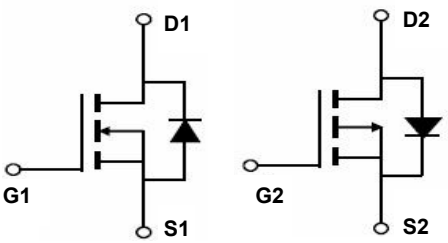
- N-Channel: 30V 30A
  $R_{DS(on)Typ}$= 7mΩ@V_{GS} = 10 V
  $R_{DS(on))Typ}$= 11mΩ@V_{GS} = 4.5V
- P-Channel: -30V- 35A
  $R_{DS(on))Typ}$= 11.3mΩ@V_{GS} = -10 V
  $R_{DS(on))Typ}$=15.5mΩ@V_{GS} = -4.5V
- Very Low On-resistance $R_{DS(ON)}$
- Low Crss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Application

☑ PWM Application
☑ Load Switch
☑ Power Management



DFN5*6 -Double base



N-Channel P-Channel

Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	30	-30	V
I_D	Drain Current - Continuous (T_C = 25℃)	30	-35	A
	- Continuous (T_C = 100℃)	20	-23	A
I_{DM}	Drain Current - Pulsed (Note 1)	120	-140	A
V_{GSS}	Gate-Source Voltage	±20	±20	V
P_D	Power Dissipation (T_C = 25℃)	17		W
$R_{\theta Jc}$	Thermal Resistance, Junction to Case	7.2		℃/W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		℃

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLM30L03T	SLM30L03T	DFN5*6 Double base	Tape & Reel	5000	25000

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =30 V, V_{GS} = 0 V	--	--	1	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D =250 uA	1.0	1.5	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 15A	--	7	8.5	mΩ
		V_{GS} = 4.5 V, I_D = 15A	-	11	13	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	--	1116	-	pF
C_{oss}	Output Capacitance		--	187	-	pF
C_{rss}	Reverse Transfer Capacitance		--	152	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{GS}= 10 V, V_{DS}= 15 V, R_G = 3 Ω ,I_D=15A	--	15	--	ns
t_r	Turn-On Rise Time		--	19	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	--	ns
t_f	Turn-Off Fall Time		--	21	--	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D =15A, V_{GS} = 10V	--	13.3	--	nC
Q_{gs}	Gate-Source Charge		--	3.1	--	nC
Q_{gd}	Gate-Drain Charge		--	5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	30	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	120	A
V_{SD}	Drain to Source Diode Forward Voltage,V_{GS} = 0V, I_{SD} =30A,T J = 25℃	--	--	1.2	V
t_{rr}	Body Diode Reverse Recovery Time ;I_F =30A,dI/dt=100A/μs	--	14	--	ns
Q_{rr}	Body Diode Reverse Recovery Charge; I_F =30A,dI/dt=100A/μs	--	4.1	--	nC

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T_J =25℃, V_{DD} =20V, V G =10V, RG =25Ω, L=0.5mH.
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 uA	-30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =-30 V, V_{GS} = 0 V	--	--	-1	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D =- 250 uA	-1.0	-1.5	-2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -8A	--	11.3	13.5	mΩ
		V_{GS} = -4.5 V, I_D = -4A	-	15.5	17.5	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz	--	2800	-	pF
C_{oss}	Output Capacitance		--	346	-	pF
C_{rss}	Reverse Transfer Capacitance		--	319	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{GS}= -10 V, V_{DS}= -15 V, R_G = 2.5 Ω ,I_D=-20A	--	14	--	ns
t_r	Turn-On Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	95	--	ns
t_f	Turn-Off Fall Time		--	65	--	ns
Q_g	Total Gate Charge	V_{DS} = -15 V, I_D =-20A, V_{GS} = -10V	--	30	--	nC
Q_{gs}	Gate-Source Charge		--	5.3	--	nC
Q_{gd}	Gate-Drain Charge		--	7.6	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-35	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-140	A
V_{SD}	Drain to Source Diode Forward Voltage,V_{GS} = 0V, I_{SD} =-10A,T J = 25°C		--	--	-1.2	V

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T_J =25℃, V DD =20V, V G =-10V, RG =25Ω, L=0.5mH,.
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

N- Channel Typical Characteristics

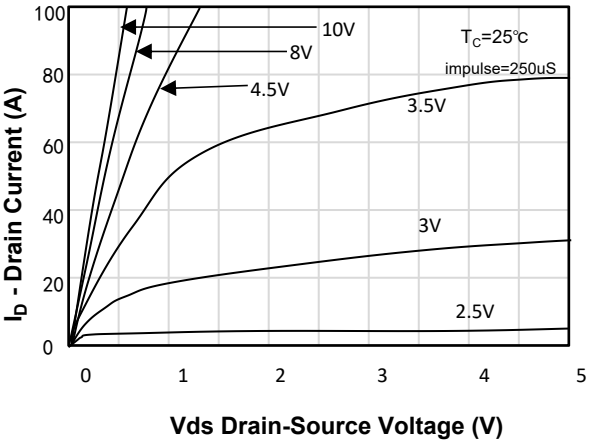


Figure 1. On-Region Characteristics

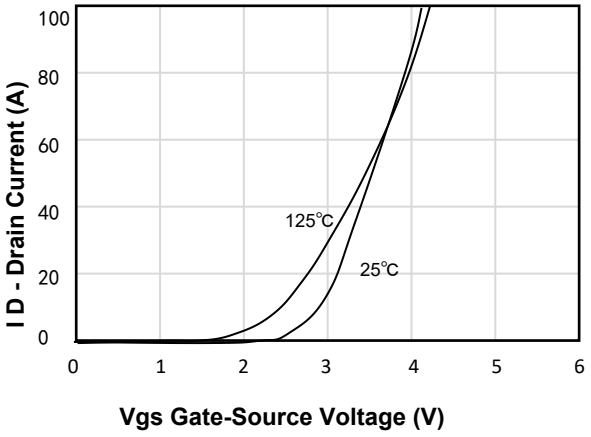


Figure 2. Transfer Characteristics

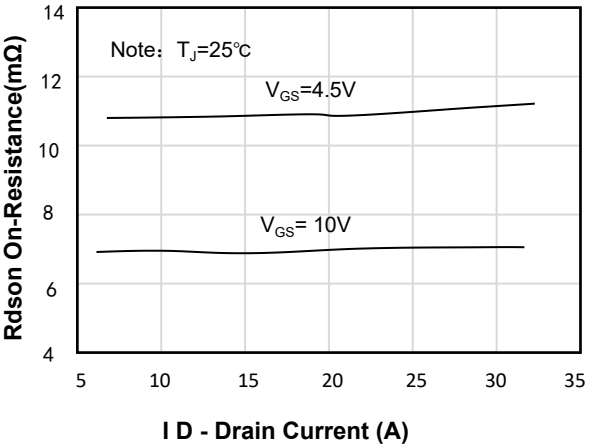


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

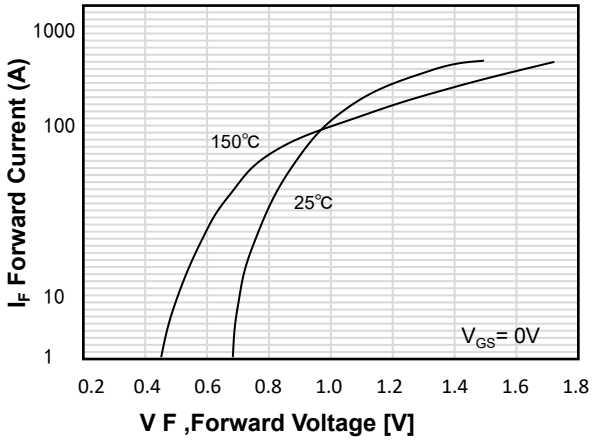


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

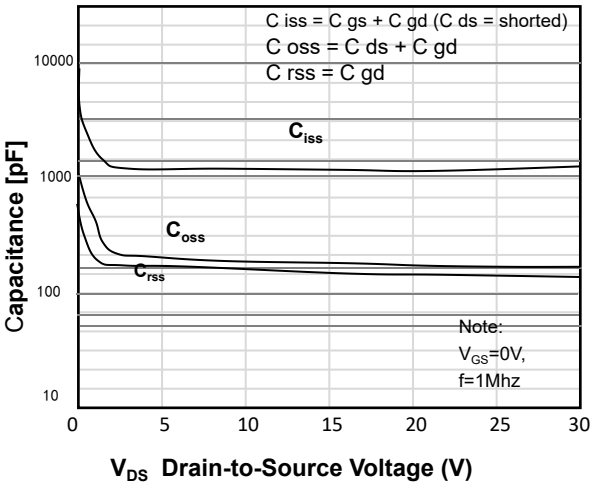


Figure 5. Capacitance Characteristics

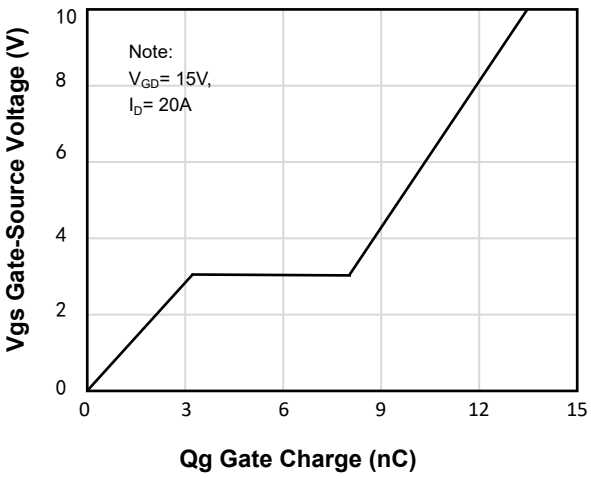


Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

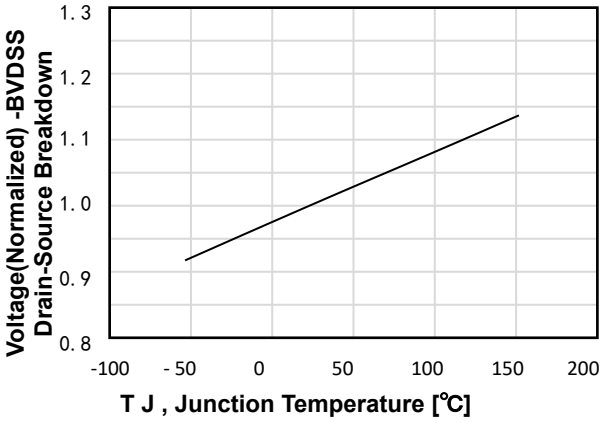


Figure 7. Breakdown Voltage Variation vs Temperature

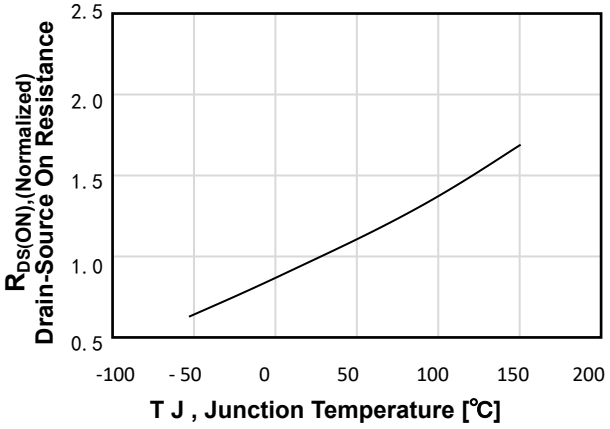


Figure 8. On-Resistance Variation vs Temperature

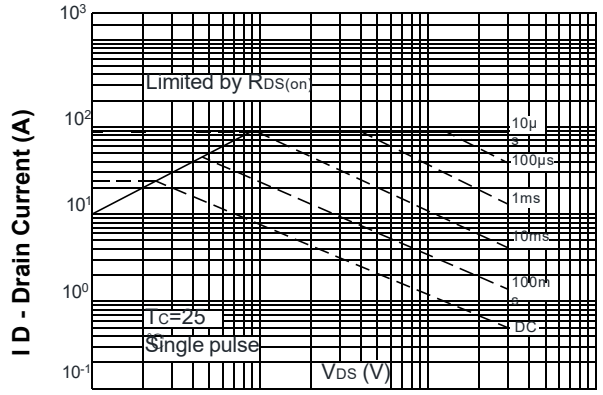


Figure 9. Maximum Safe Operating Area

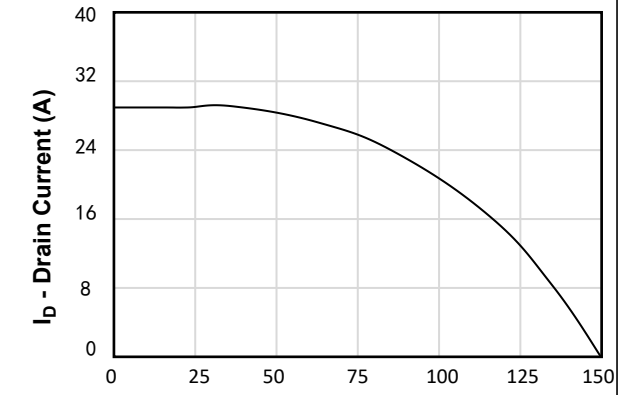


Figure 10. Maximum Continuous Drain Current vs Temperature

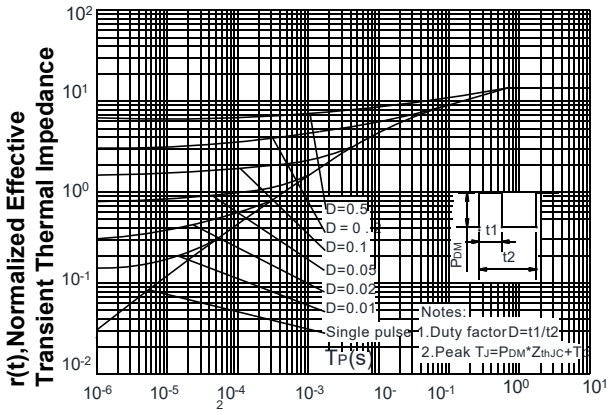
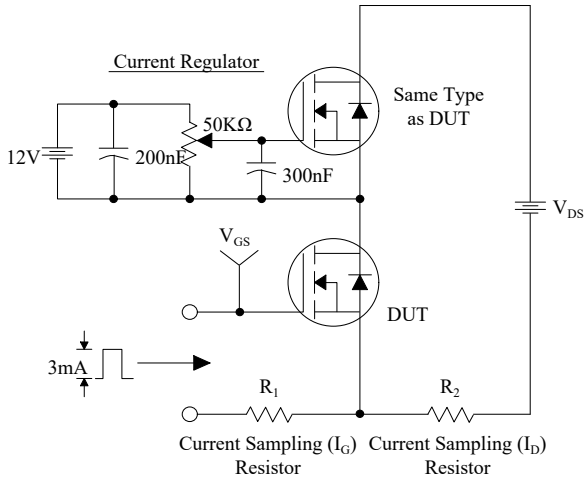
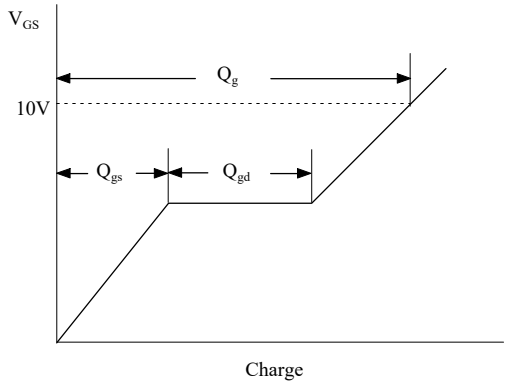


Figure 11. Transient Thermal Response Curve

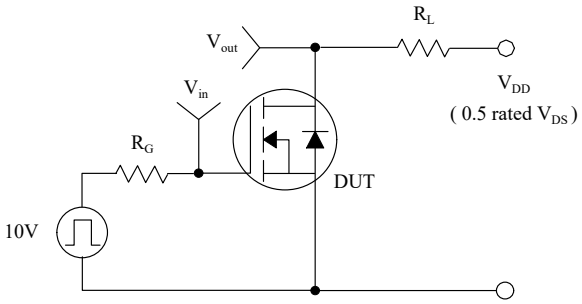
N- Channel

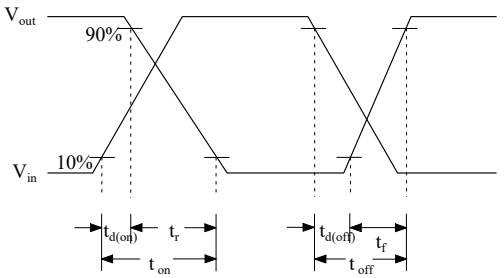
Gate Charge Test Circuit & Waveform



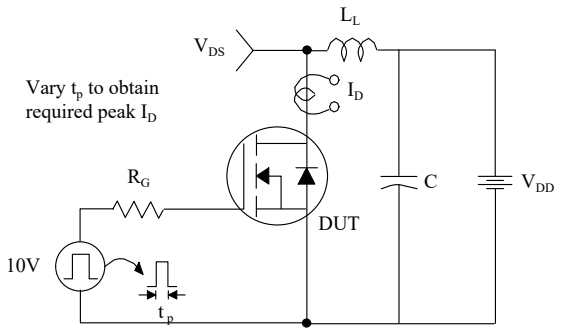


Resistive Switching Test Circuit & Waveforms

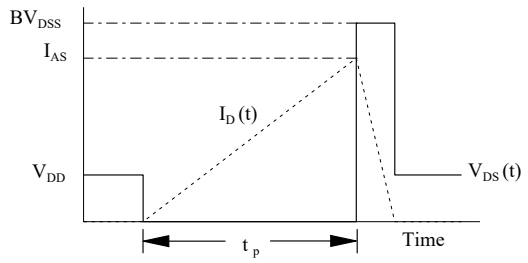




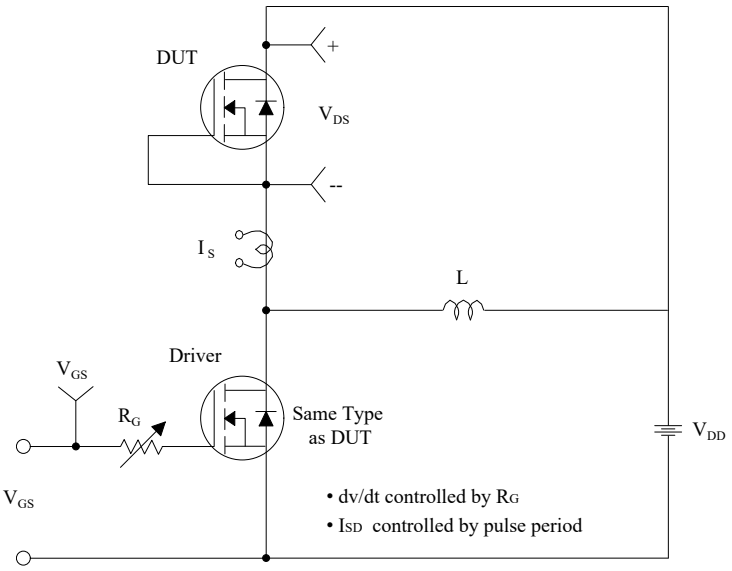
Unclamped Inductive Switching Test Circuit & Waveforms

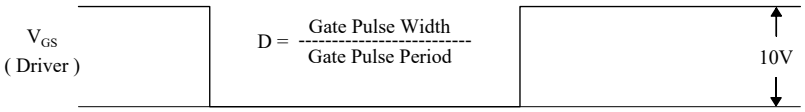


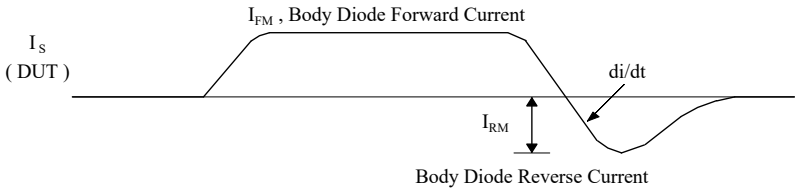
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$

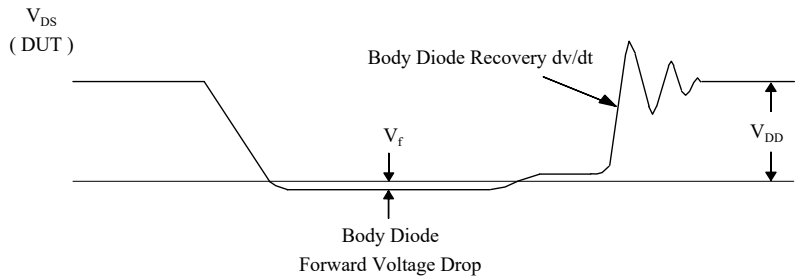


N- Channel Peak Diode Recovery dv/dt Test Circuit & Waveforms









P- Channel Typical Characteristics

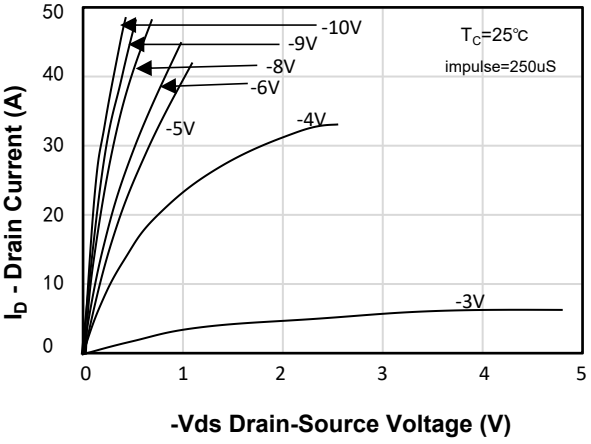


Figure 1. On-Region Characteristics

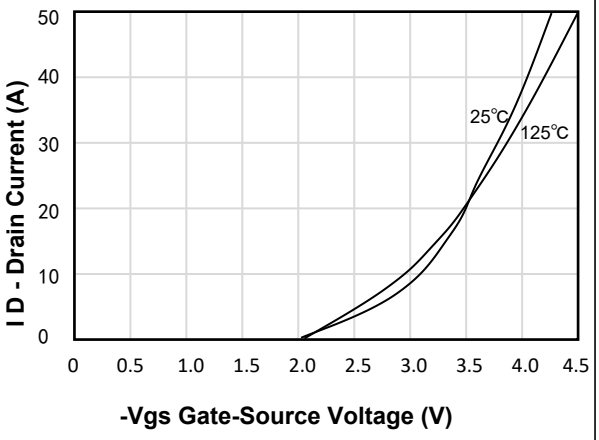


Figure 2. Transfer Characteristics

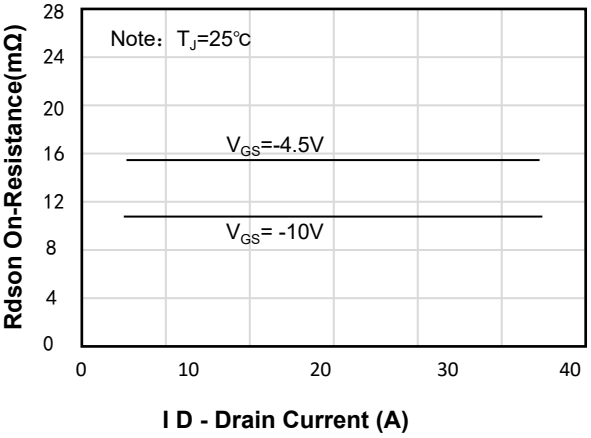


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

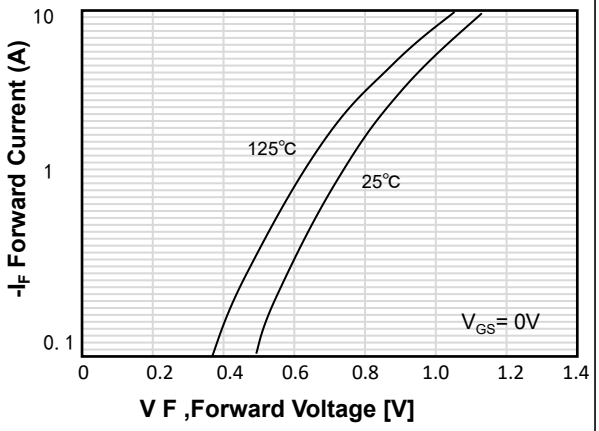


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

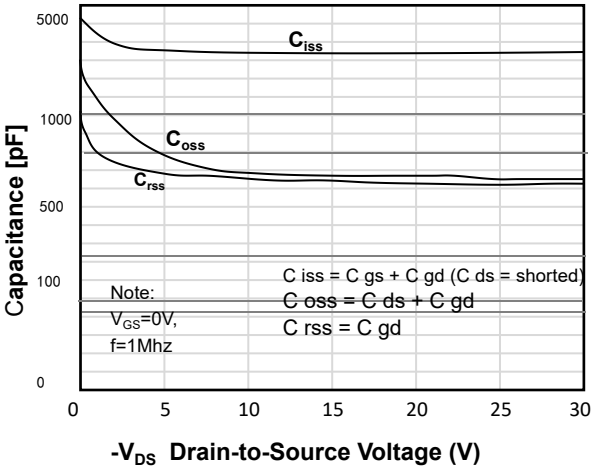


Figure 5. Capacitance Characteristics

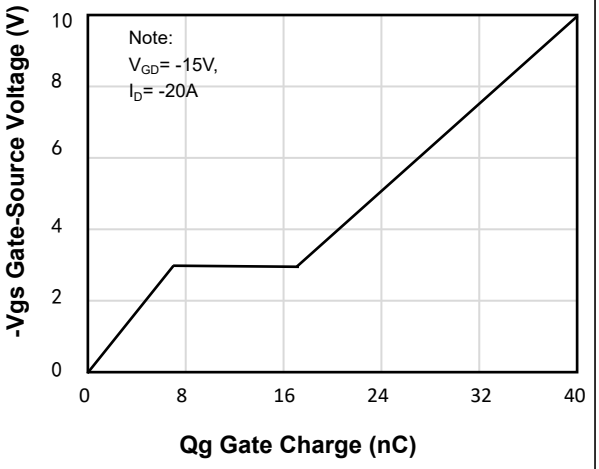


Figure 6. Gate Charge Characteristics

P- Channel Typical Characteristics (Continued)

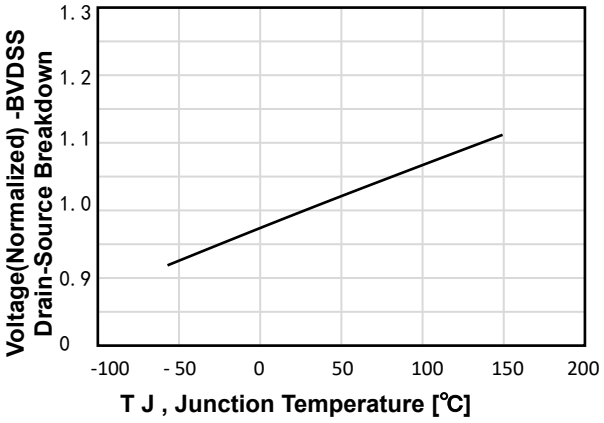


Figure 7. Breakdown Voltage Variation vs Temperature

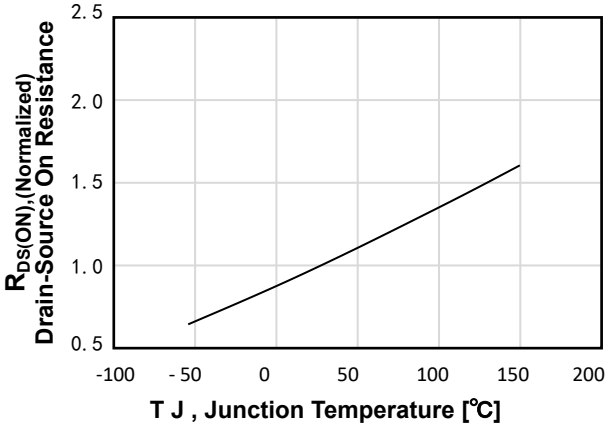


Figure 8. On-Resistance Variation vs Temperature

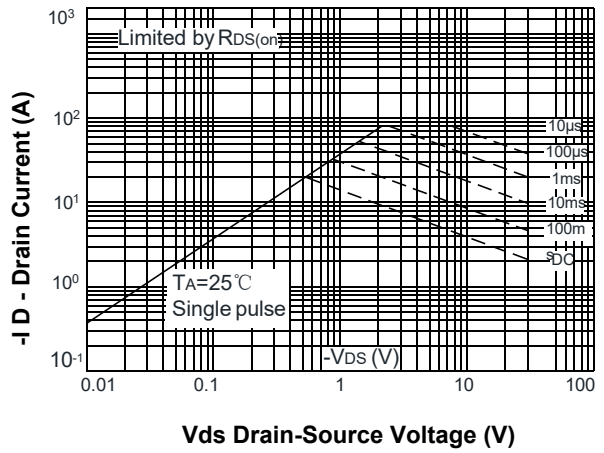


Figure 9. Maximum Safe Operating Area

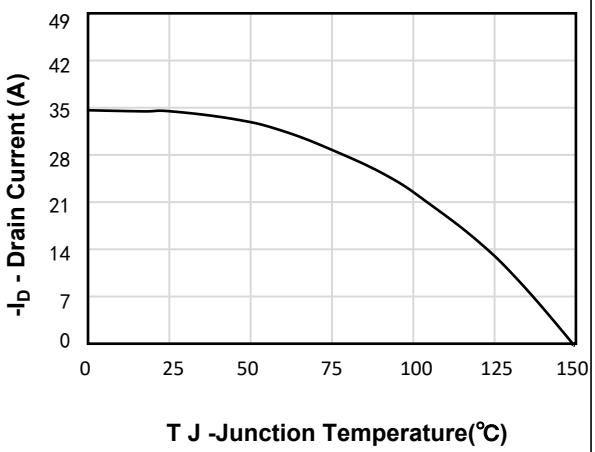


Figure 10. Maximum Continuous Drain Current vs Temperature

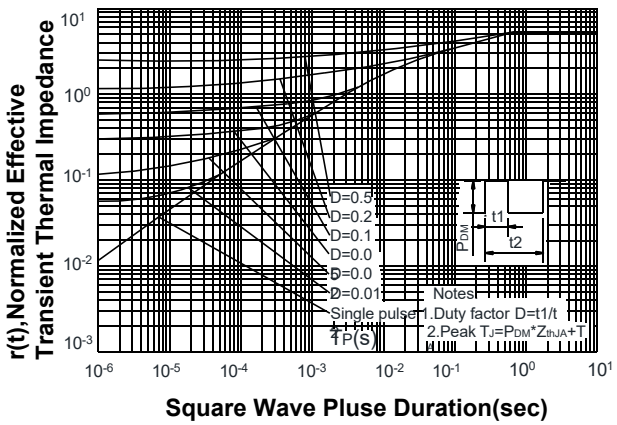
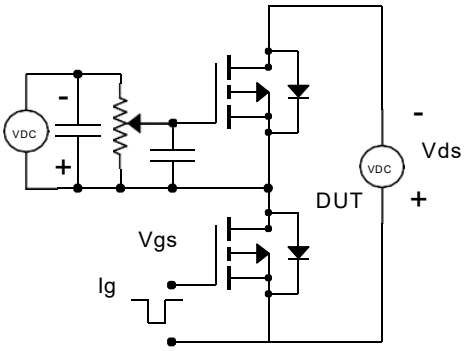
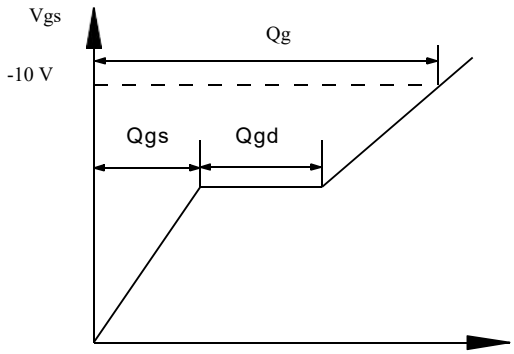


Figure 11. Transient Thermal Response Curve

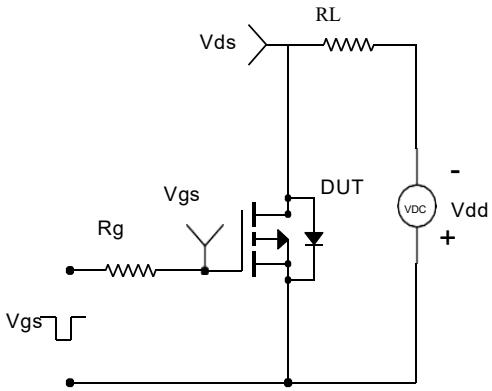
P- Channel

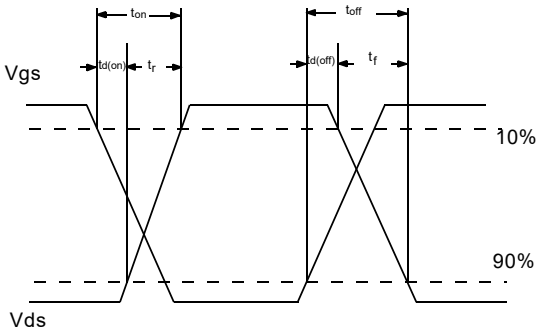
Gate Charge Test Circuit & Waveform



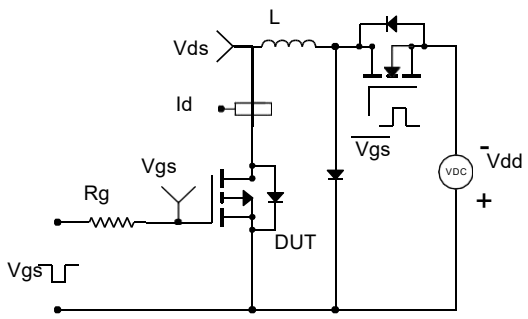


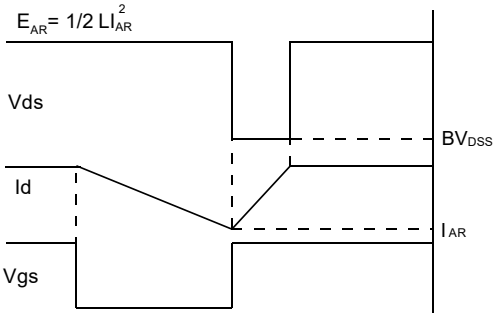
Resistive Switching Test Circuit & Waveforms





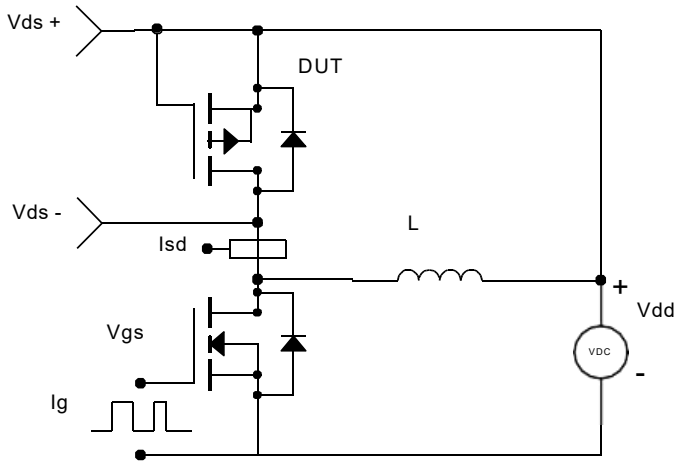
Unclamped Inductive Switching Test Circuit & Waveforms



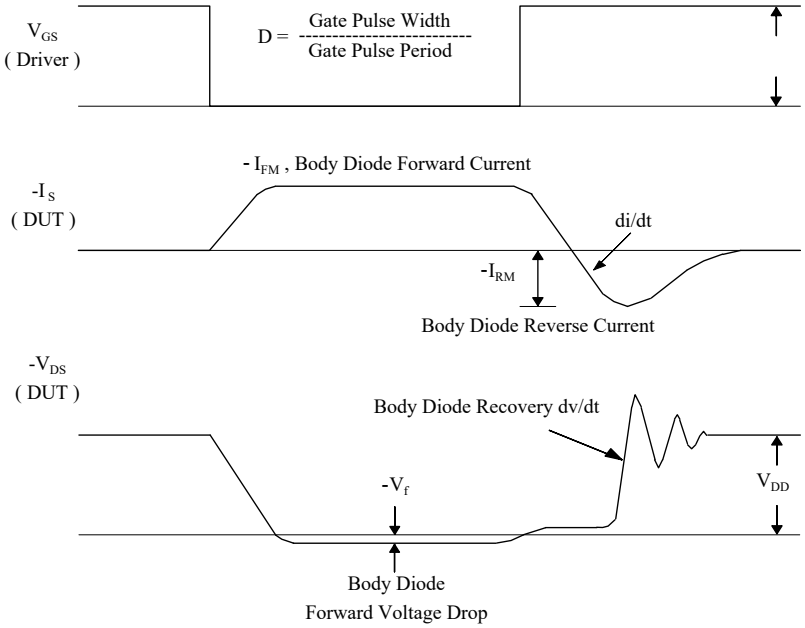


P- Channel

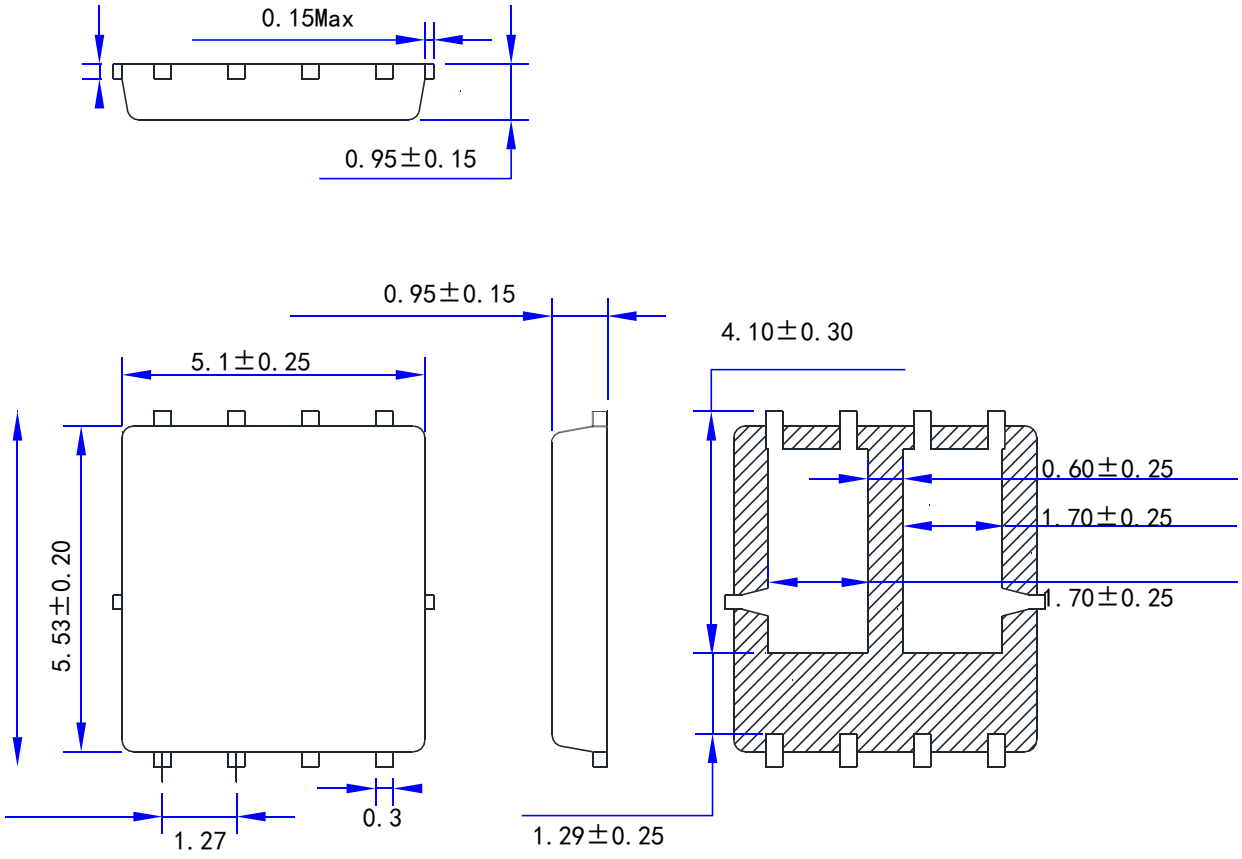
Peak Diode Recovery dv/dt Test Circuit & Waveforms



- dv/dt controlled by R_G
- I_{SD} controlled by pulse period



DFN 5*6 Double Base OUTLINE



NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.15,Unmarked filletRmax=0.25

NAME	DFN5*6-Double OUTLINE	UNIT	mm	DESIGNED	Shawn Chen	THIRD ANGLE SYSTEM
DWGNO		PAGE	1 OF 1	CHECKED		
VERSION	Ver1.0	ISSUE DATE		APPROVED		

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