美浦森半导体
M s e m i t e k

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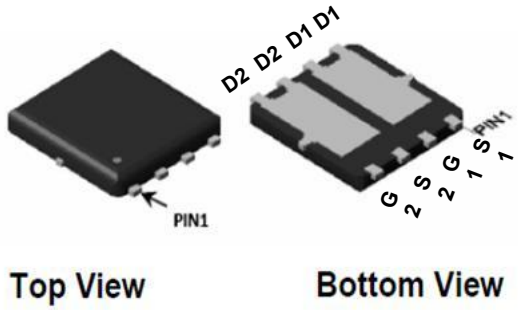
SLM50D06T
60V N-Channel MOSFET

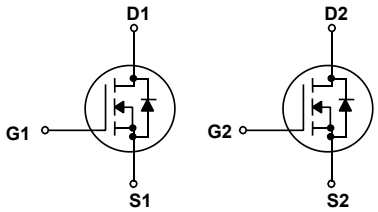
General Description

This Power MOSFET is produced using Msemitek's advanced TRENCH technology.
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Application
☑PWM Application
☑Load Switch
☑Power Management

Features
- N-Channel:60V 50A
  $R_{DS(on)Typ}$= 14.8mΩ@VGS = 10 V
  $R_{DS(on)Typ}$= 18.2mΩ@VGS = 4.5 V
- Very Low On-resistance $R_{DS(ON)}$
- Low Crss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	SLM50D06T	Units
V_{DSS}	Drain-Source Voltage	60	V
I_D	Drain Current - Continuous (T_C = 25℃)	50	A
	- Continuous (T_C = 100℃)	33	A
I_{DM}	Drain Current - Pulsed (Note 1)	200	A
V_{GSS}	Gate-Source Voltage	±30	V
EAS	Single Pulsed Avalanche Energy (Note 2)	156	mJ
E_{AR}	Repetitive Avalanche Energy (Note 1)	12	mJ
P_D	Power Dissipation (T_C = 25℃)	89	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	℃

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLM50D06T	SLM50D06T	PDFN5*6	Tape & Reel	5000	50000

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	60	--	--	V
$\triangle BV_{DSS}$ / $\triangle T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 uA, Referenced to 25℃	--	0.06	--	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 48 V, T_C = 150℃	--	--	10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	1.0	--	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 20 A	--	14.8	16	mΩ
		V_{GS} = 4.5 V, I_D = 20 A	--	18.2	24	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	2780	--	pF
C_{oss}	Output Capacitance		--	112	--	pF
C_{rss}	Reverse Transfer Capacitance		--	103	--	pF
Switching Characteristics						
$t_{d(on)3}$	Turn-On Delay Time	V_{DD} = 30 V, I_D = 25 A, R_G = 25 Ω (Note 3)	--	15	--	ns
t_r	Turn-On Rise Time		--	105	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	60	--	ns
t_f	Turn-Off Fall Time		--	65	--	ns
Q_g	Total Gate Charge	V_{DS} = 30 V, I_D = 20 A, V_{GS} = 4.5 V (Note 3)	--	26.6	--	nC
Q_{gs}	Gate-Source Charge		--	7.7	--	nC
Q_{gd}	Gate-Drain Charge		--	11.2	--	nC
R_G	Gate Resistance	f = 1MHz	--	-	--	Ω
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	50	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	200	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 50 A	--	--	1.4	V

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T_J =25℃, V_{DD} = 20V, V_G = 10V, L=0.5mH.
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

N- Channel Typical Characteristics

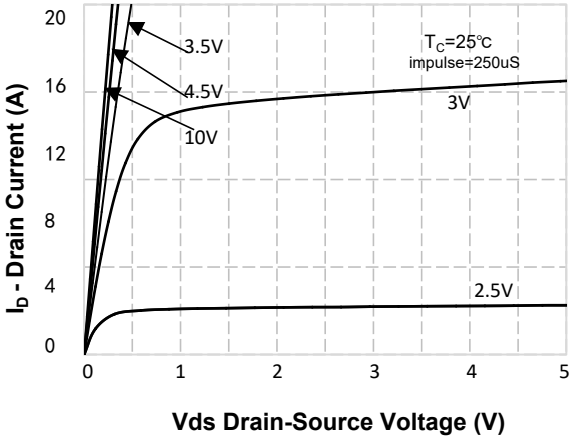


Figure 1. On-Region Characteristics

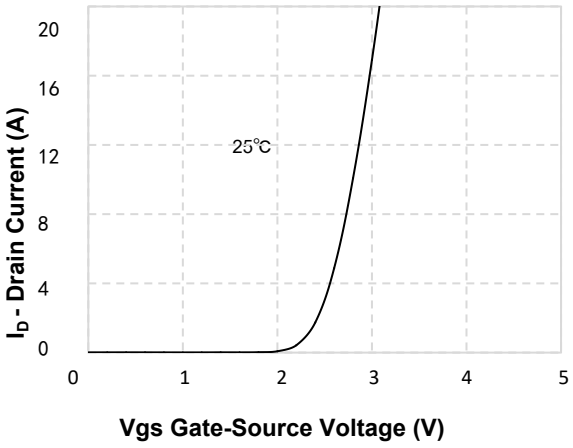


Figure 2. Transfer Characteristics

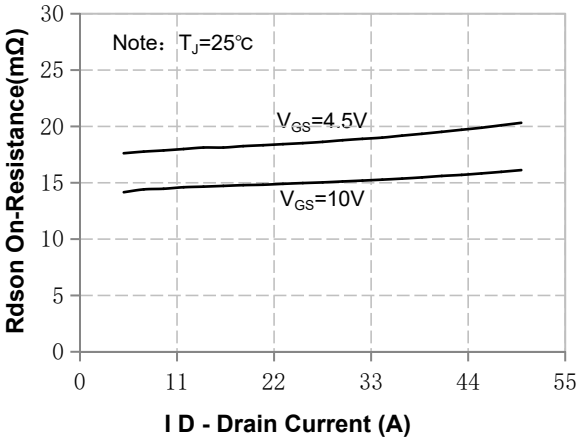


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

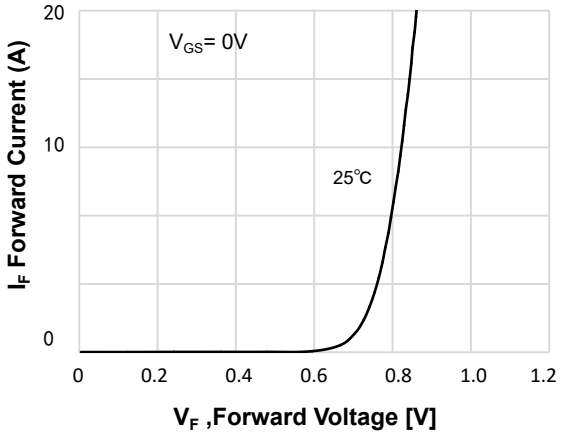


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

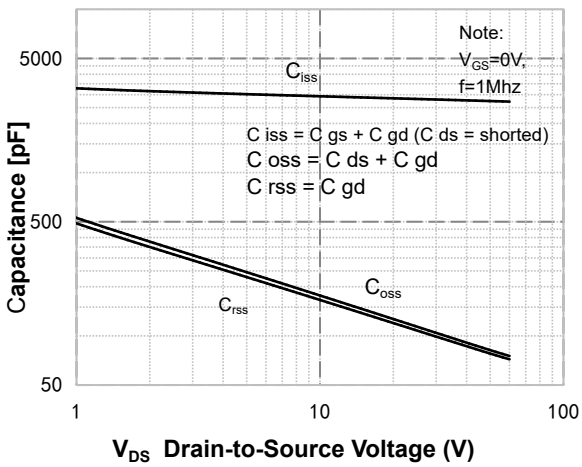


Figure 5. Capacitance Characteristics

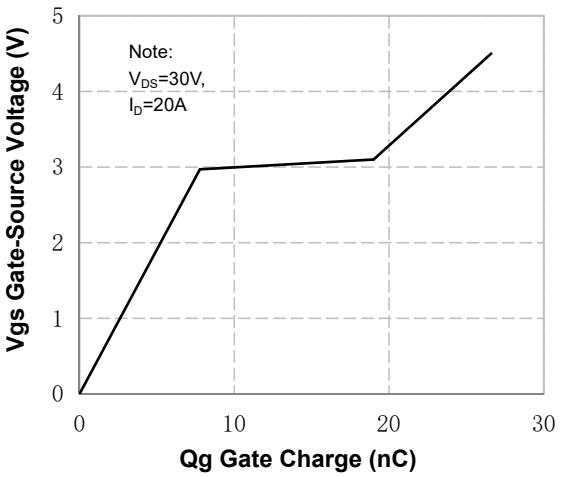


Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

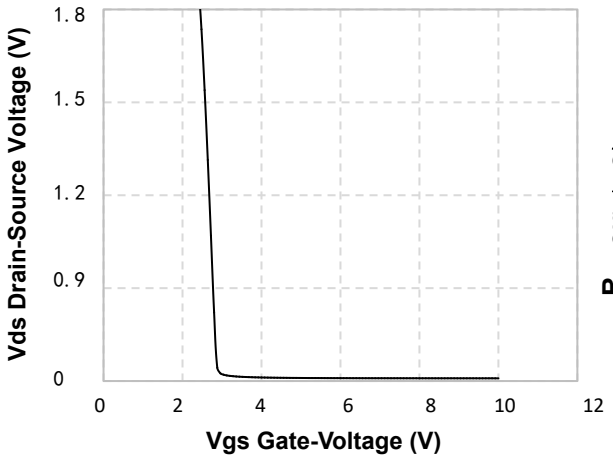


Figure 7. Vds Drain-Source Voltage vs Gate Voltage

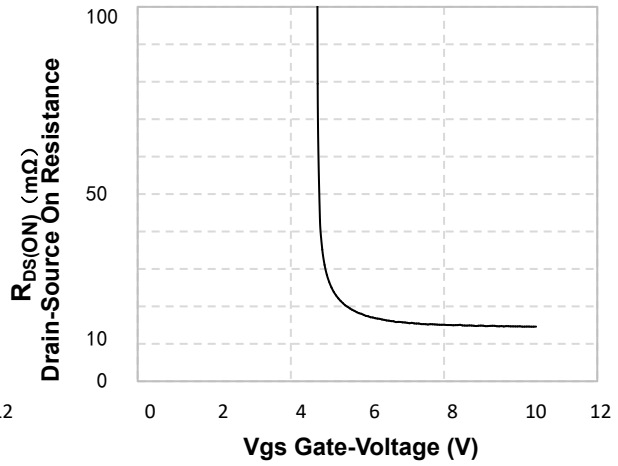


Figure 8. On-Resistance vs Gate Voltage

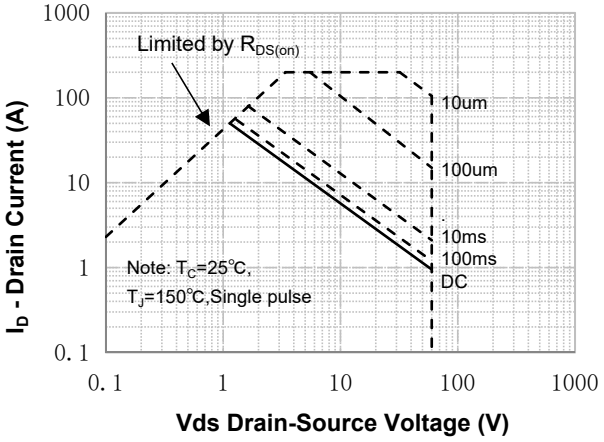


Figure 9. Maximum Safe Operating Area

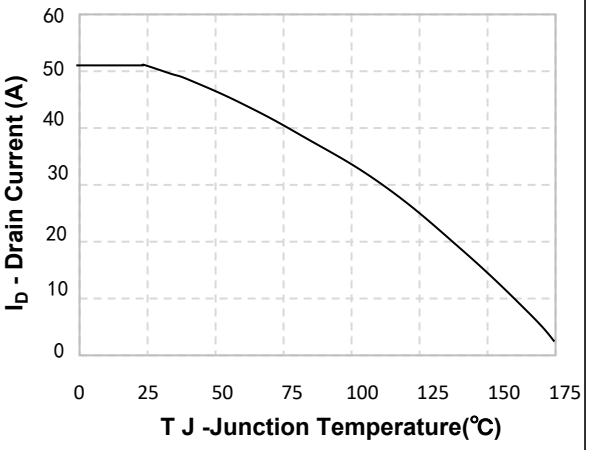


Figure 10. Maximum Continuous Drain Current vs Temperature

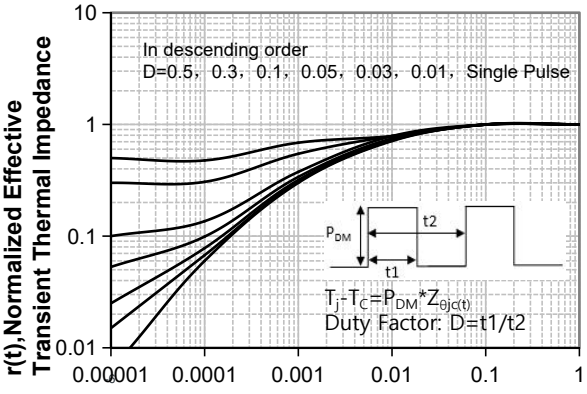
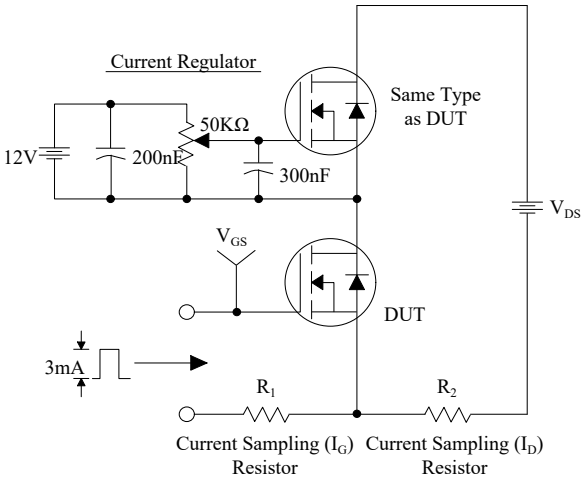
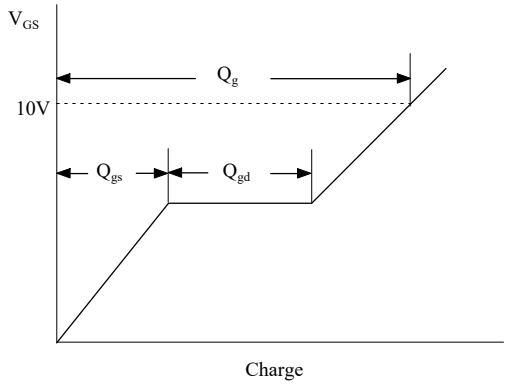


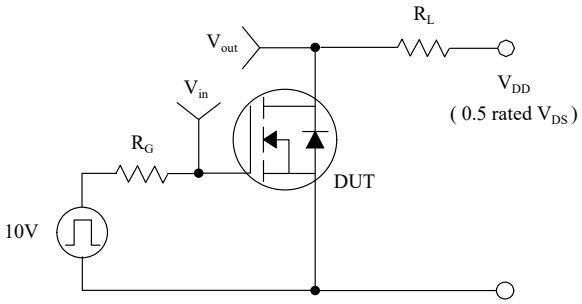
Figure 11. Transient Thermal Response Curve

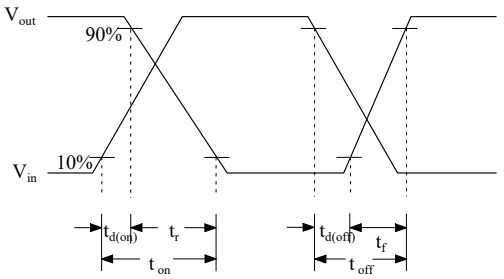
Gate Charge Test Circuit & Waveform



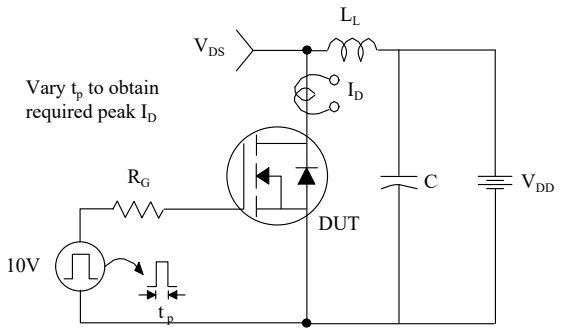


Resistive Switching Test Circuit & Waveforms

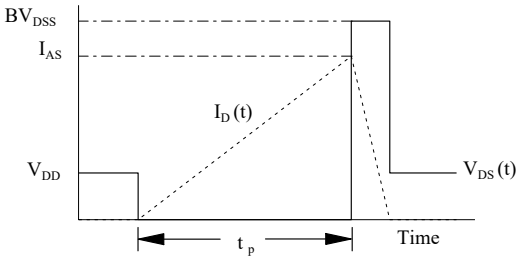




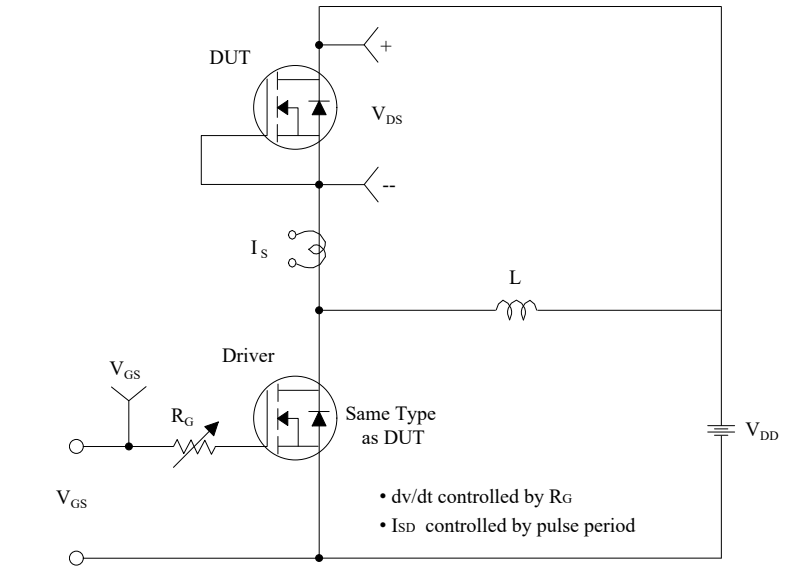
Unclamped Inductive Switching Test Circuit & Waveforms

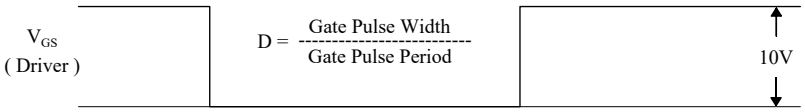


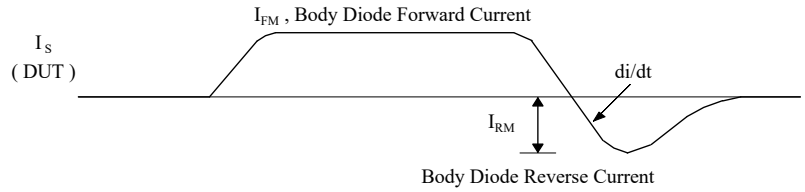
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

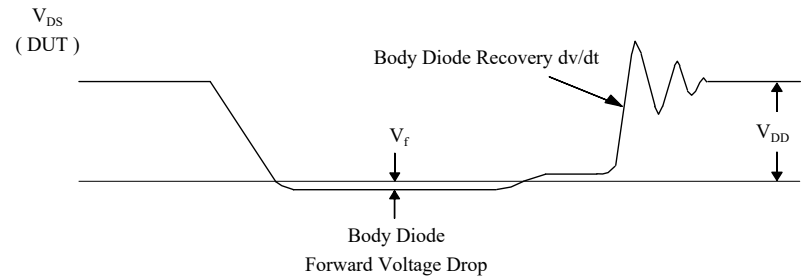


Peak Diode Recovery dv/dt Test Circuit & Waveforms

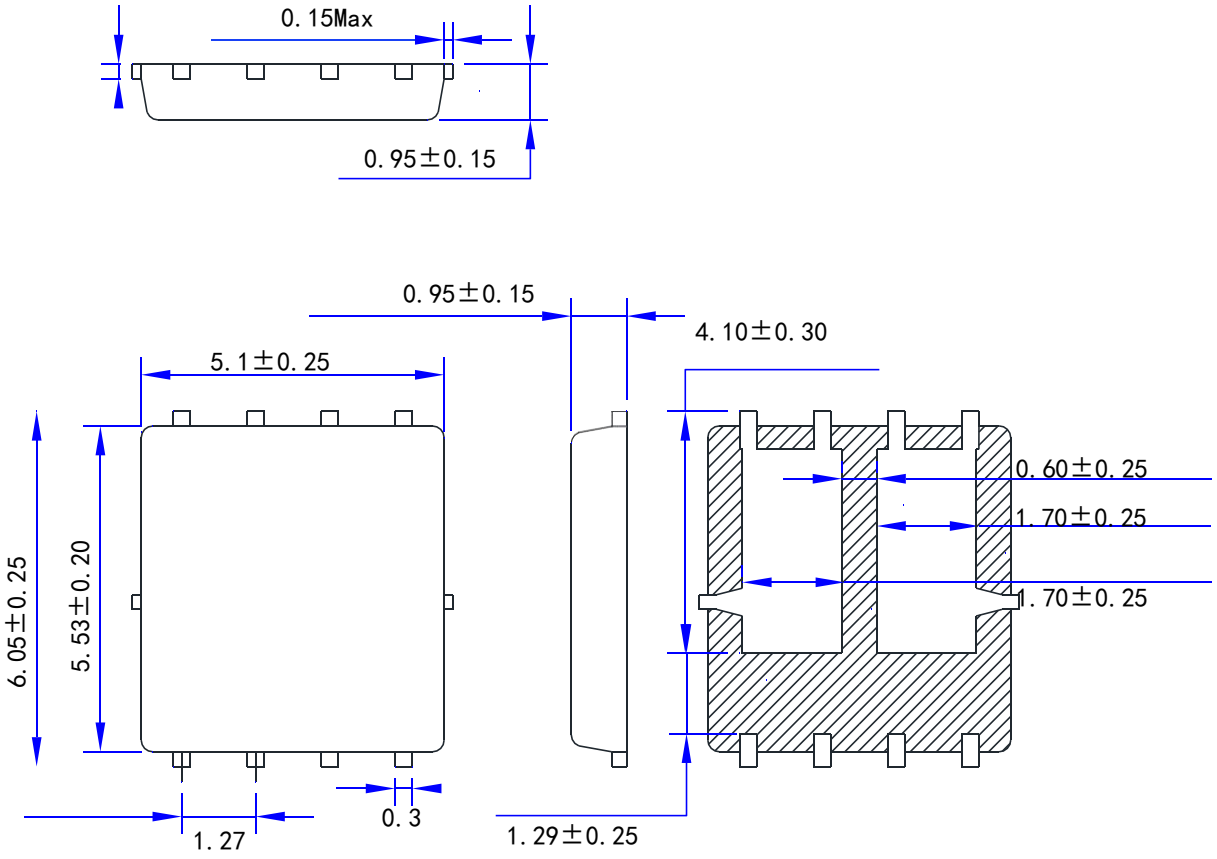








DFN 5*6 Double Base OUTLINE



NOTE:
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.15,Unmarked filletRmax=0.25

NAME	DFN5*6-Double OUTLINE	UNIT	mm	DESIGNED	Shawn Chen	THIRD ANGLE SYSTEM
DWGNO		PAGE	1 OF 1	CHECKED		
VERSION	Ver1.0	ISSUE DATE		APPROVED		

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