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SLD50P06T
# 60V P -Channel MOSFET

General Description
This Power MOSFET is produced using Msemitek's advanced TRENCH technology.
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Application
☑ PWM Application
☑ Load Switch
☑ Power Management

Features
- P-Channel:-60V -50A
  $R_{DS(on)Typ}$= 25mΩ@VGS = -10 V
  $R_{DS(on)Typ}$= 27mΩ@VGS = -4.5 V
- Very Low On-resistance $R_{DS(ON)}$
- Low Crss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

D-PAK
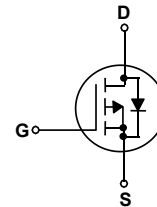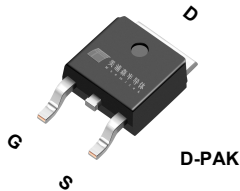
Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		SLD50P06T	Units
V_{DSS}	Drain-Source Voltage		-60	V
I_D	Drain Current - Continuous (T_C = 25°C)		-50	A
	- Continuous (T_C = 100°C)		-31	A
I_{DM}	Drain Current - Pulsed	(Note 1)	-200	A
V_{GSS}	Gate-Source Voltage		±20	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	225	mJ
P_D	Power Dissipation (T_C = 25°C)		57	W
$R_{θJC}$	Thermal Resistance, Junction to Case		2.2	°C/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLD50P06T	SLD50P06T	TO-252	Tape & Reel	2500	25000

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 uA	-60	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =-60 V, V_{GS} = 0 V	--	--	-1	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 uA	-1.0	-1.7	-2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} =-10 V, I_D = -20A	--	25	29	mΩ
		V_{GS} =-4.5 V, I_D = -20A	--	27	31	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -20 V, V_{GS} = 0 V, f = 1.0 MHz	--	3780	-	pF
C_{oss}	Output Capacitance		--	195	-	pF
C_{rss}	Reverse Transfer Capacitance		--	160	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=-10V, V_{DS}=-15V, (Note 3) R_G = 3.3Ω ,I_D=-1A Tj=25℃	--	39	--	ns
t_r	Turn-On Rise Time		--	24	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	102	--	ns
t_f	Turn-Off Fall Time		--	7	--	ns
Q_g	Total Gate Charge	V_{DS} =-20V, I_D =-12A, (Note 3) V_{GS} = -10V	--	52	--	nC
Q_{gs}	Gate-Source Charge		--	7.4	--	nC
Q_{gd}	Gate-Drain Charge		--	6.5	--	nC
R_G	Gate Resistance	f = 1MHz	--	6.1	--	Ω
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-50	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-200	A
V_{SD}	Drain to Source Diode Forward Voltage,V_{GS} = 0V, I_{SD} =-20A,T_J = 25℃		--	--	-1.2	V

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T_J =25℃, V_{DD} = -20V, V_G = -10V, L=0.5mH.
3. Pulse Test: Pulse Width≤300µs, Duty Cycle≤0.5%

P- Channel Typical Characteristics
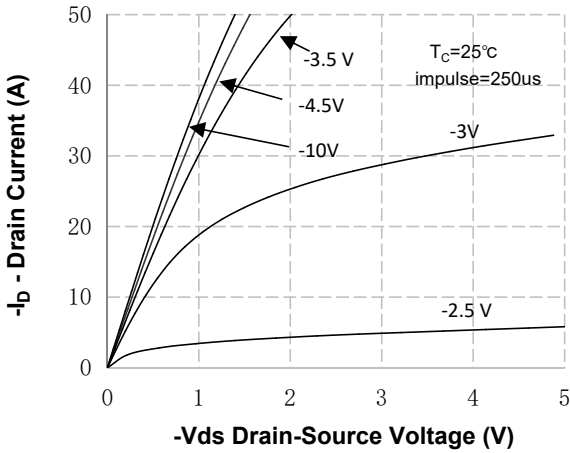
Figure 1. On-Region Characteristics

- Axes: $-I_D$ - Drain Current (A) vs -Vds Drain-Source Voltage (V)
- Curves labeled: -3.5 V, -4.5V, -10V, -3V, -2.5 V
- T_C=25℃, impulse=250us
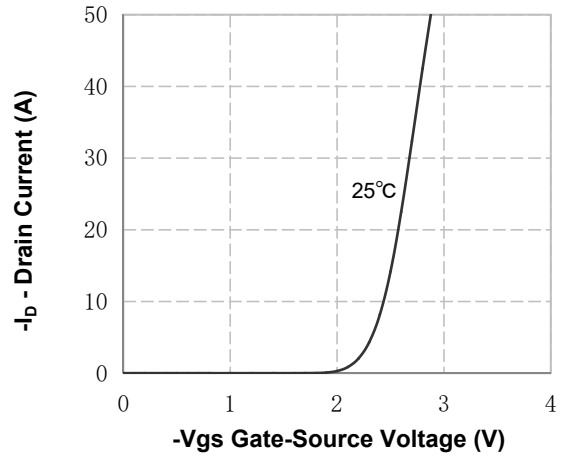
Figure 2. Transfer Characteristics

- Axes: $-I_D$ - Drain Current (A) vs -Vgs Gate-Source Voltage (V)
- 25℃
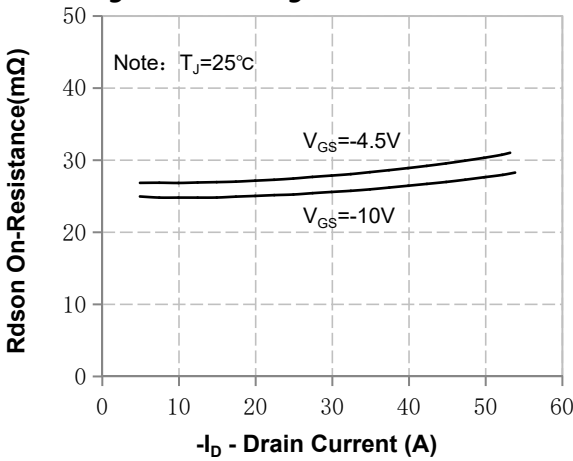
Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

- Axes: Rdson On-Resistance(mΩ) vs $-I_D$ - Drain Current (A)
- Note: T_J=25℃
- V_{GS}=-4.5V
- V_{GS}=-10V
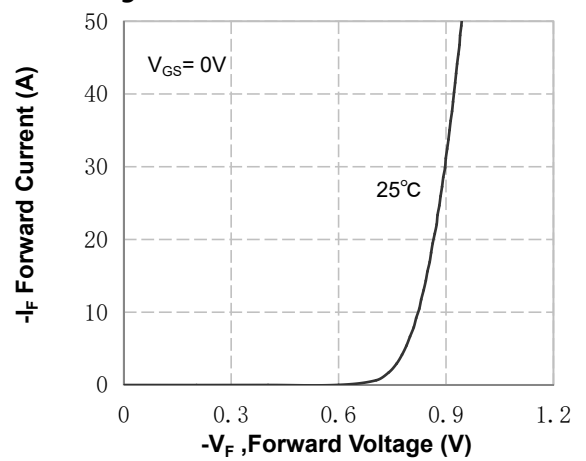
Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

- Axes: $-I_F$ Forward Current (A) vs $-V_F$,Forward Voltage (V)
- V_{GS}= 0V
- 25℃
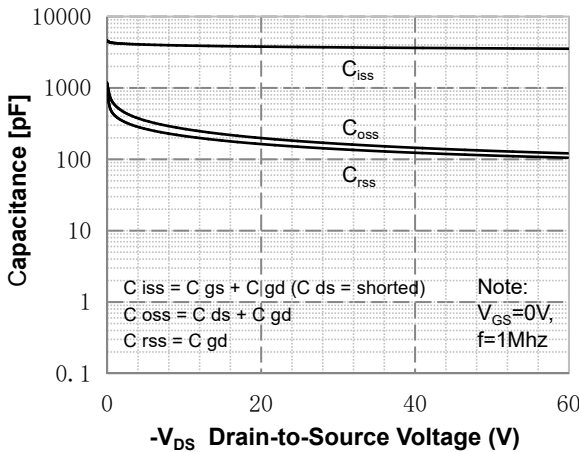
Figure 5. Capacitance Characteristics

- Axes: Capacitance [pF] vs $-V_{DS}$ Drain-to-Source Voltage (V)
- C_{iss}
- C_{oss}
- C_{rss}
- C iss = C gs + C gd (C ds = shorted)
- C oss = C ds + C gd
- C rss = C gd
- Note: V_{GS}=0V, f=1Mhz
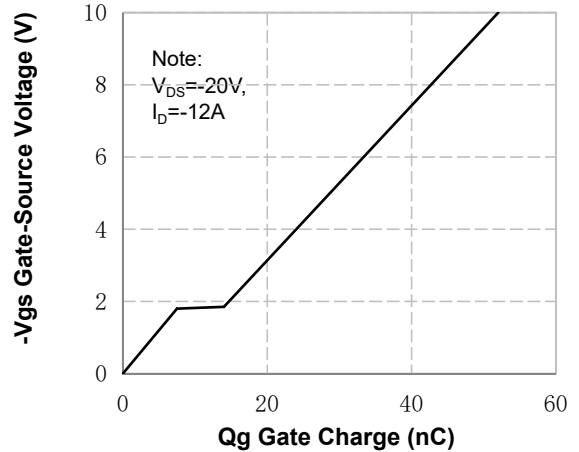
Figure 6. Gate Charge Characteristics

- Axes: -Vgs Gate-Source Voltage (V) vs Qg Gate Charge (nC)
- Note: V_{DS}=-20V, I_D=-12A

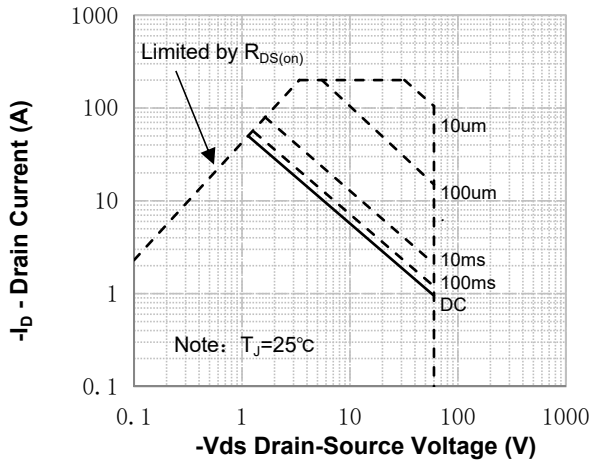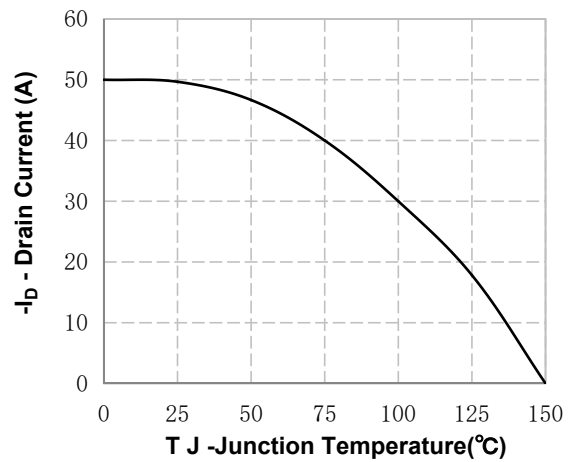# P- Channel Typical Characteristics (Continued)
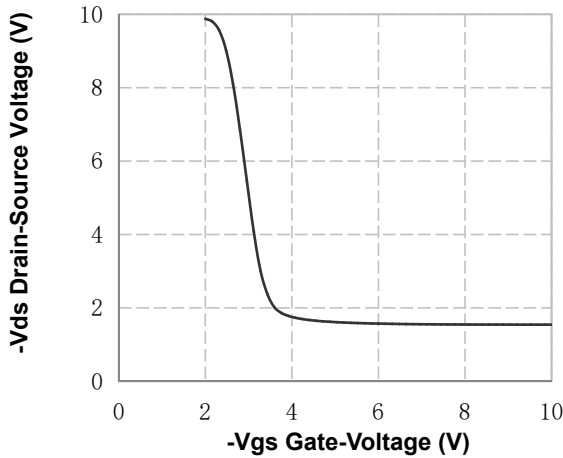
Figure 7. Vds Drain-Source Voltage
vs Gate Voltage
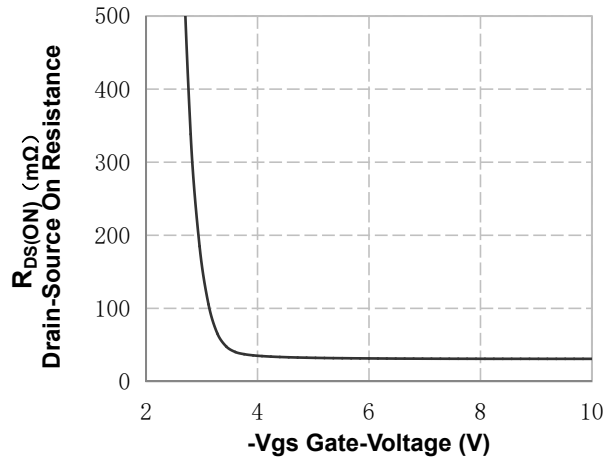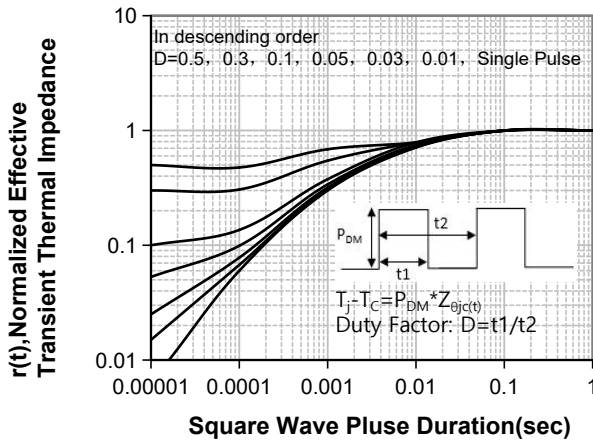
Figure 8. On-Resistance
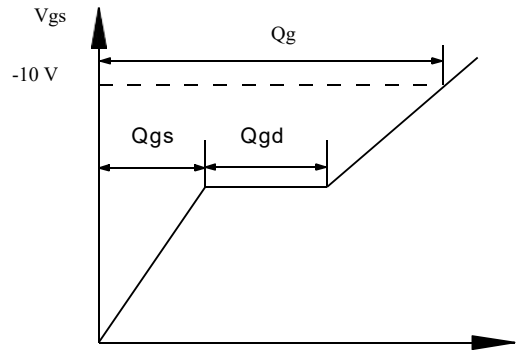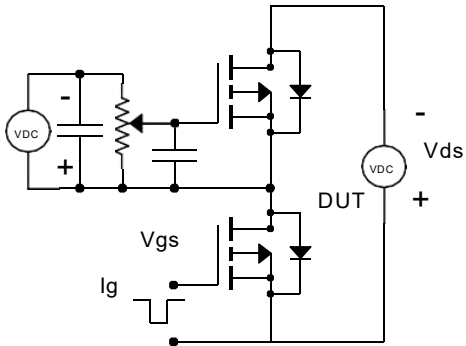vs Gate Voltage

Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Continuous Drain
Current vs Temperature

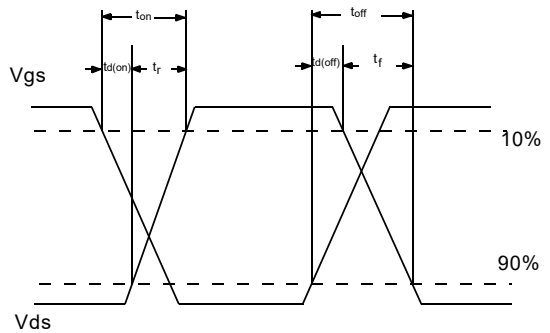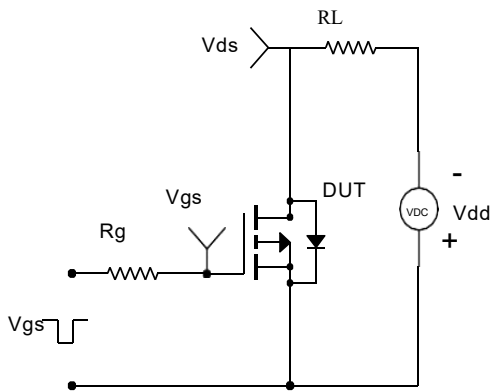Figure 11. Transient Thermal Response Curve

P- Channel

Gate Charge Test Circuit & Waveform

Vgs

-10 V

Qg

Qgs   Qgd

VDC

Vds

DUT

Vgs

Ig

Resistive Switching Test Circuit & Waveforms

RL

Vds

Rg   Vgs   DUT   Vdd

Vgs

t_on   t_off

td(on) t_r   td(off) t_f

Vgs

10%

90%

Vds

Unclamped Inductive Switching Test Circuit & Waveforms

L

Vds

Id

Rg   Vgs   Vgs   Vdd

DUT

Vgs

$E_{AR} = 1/2 \ LI_{AR}^2$

Vds

BV_{DSS}

Id

I_{AR}

Vgs
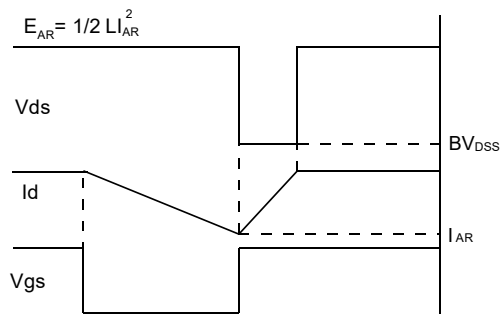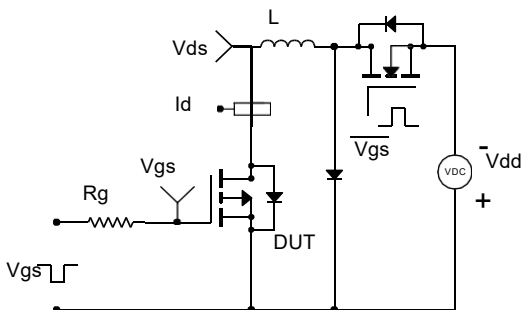
P- Channel

Peak Diode Recovery dv/dt Test Circuit & Waveforms

Vds +

DUT

Vds -

Isd

L

Vgs

+
Vdd

VDC

-

Ig
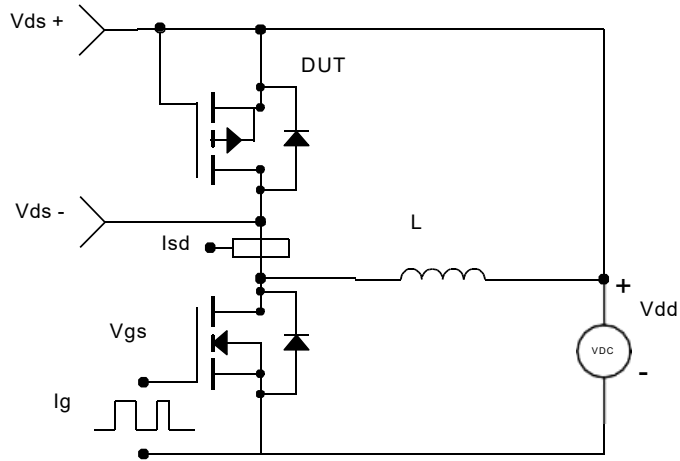
- dv/dt controlled by R_G
- I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

$-I_S$
(DUT)

$-I_{FM}$, Body Diode Forward Current

di/dt

$-I_{RM}$

Body Diode Reverse Current

$-V_{DS}$
(DUT)

Body Diode Recovery dv/dt

$-V_f$

V_{DD}

Body Diode
Forward Voltage Drop

TO-252 OUTLINE

6.60±0.20

5.32±0.20

0.852±0.15

6.10±0.20

0.85±0.20

0.80±0.20

2.286   2.286

2.30±0.20

0.508±0.05

1.00±0.10

0.508±0.05

光面

0.76±0.10

2.848±0.30
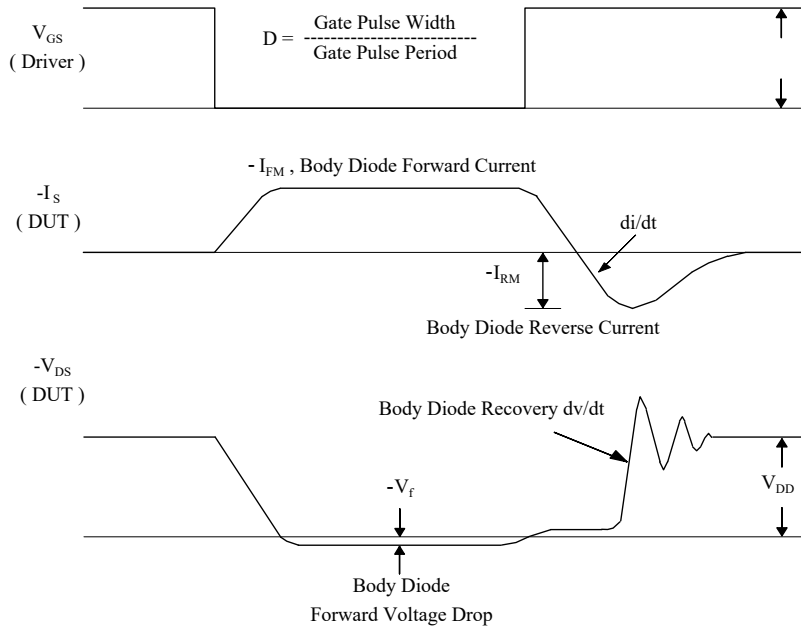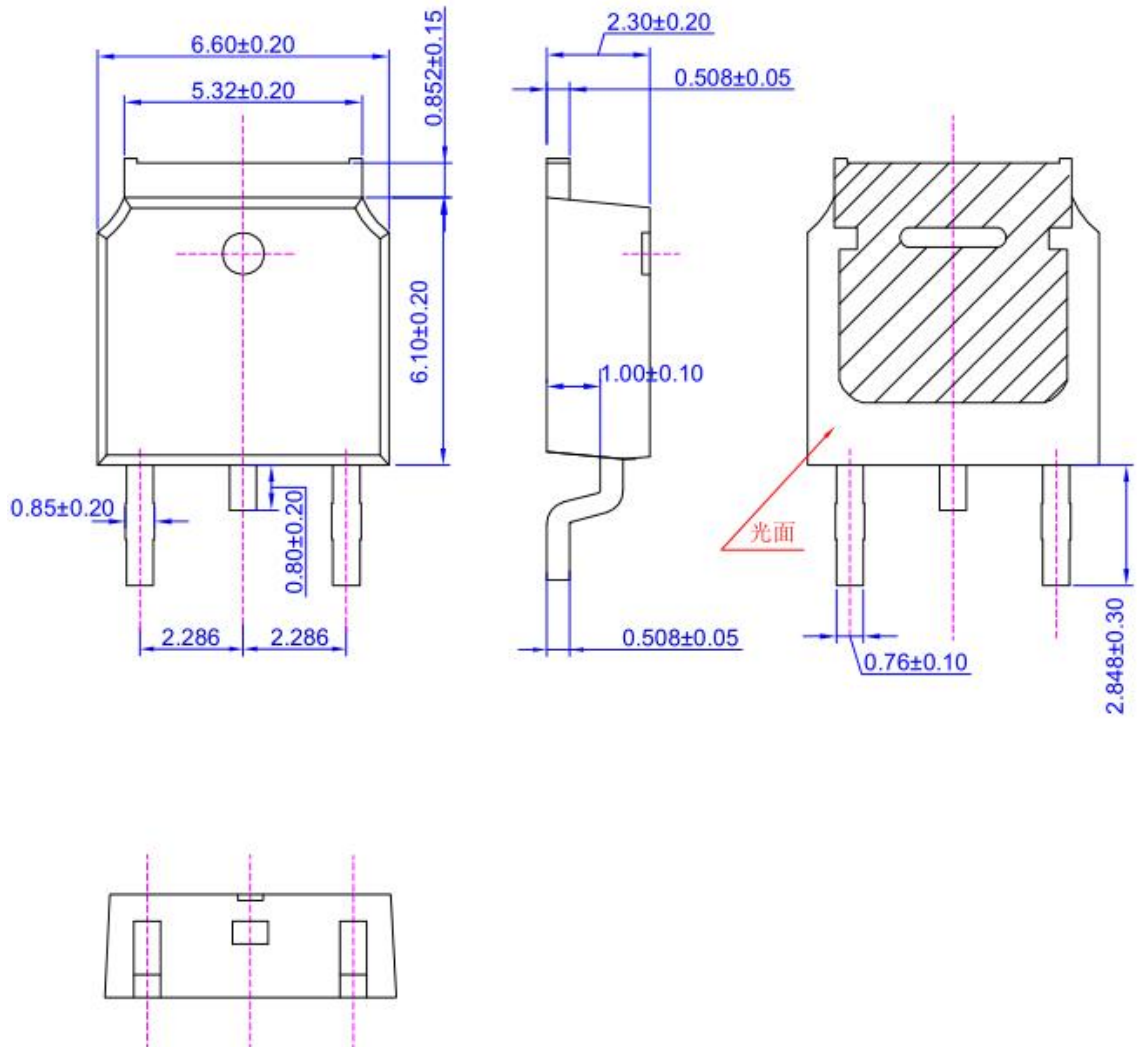
NOTE：

1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8

2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25

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