



SLF18N50C **500V N-channel MOSFET**

General Description

This Power MOSFET is produced using Msemitek's advanced planar stripe DMOS technology.

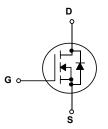
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for AC/DC power conversion in switching mode operation for higher efficiency.

Features

- 18A, 500V, $R_{DS(on)typ}$ = 212m $\Omega @V_{GS}$ = 10 V Low gate charge (typical 87nC)
- Low Crss (typical 32pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		SLF18N50C	Units
V _{DSS}	Drain-Source Voltage		500	V
	Drain Current - Continuous (T _C = 25°C)		18	Α
ID	- Continuous (T _C = 100°C)		11.7	Α
I _{DM}	Drain Current - Pulsed	(Note 1)	72	Α
V _{GSS}	Gate-Source Voltage		±30	V
EAS	Single Pulsed Avalanche Energy	(Note 2)	689	mJ
I_{AR}	Avalanche Current	(Note 1)	18	Α
E _{AR}	Repetitive Avalanche Energy		65	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	45	V/ns
P _D	Power Dissipation (T _C = 25°C)		41	W
	- Derate above 25°C		0.33	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T∟	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

^{*} Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	SLF18N50C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.04	°C/W
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	63	°C/W

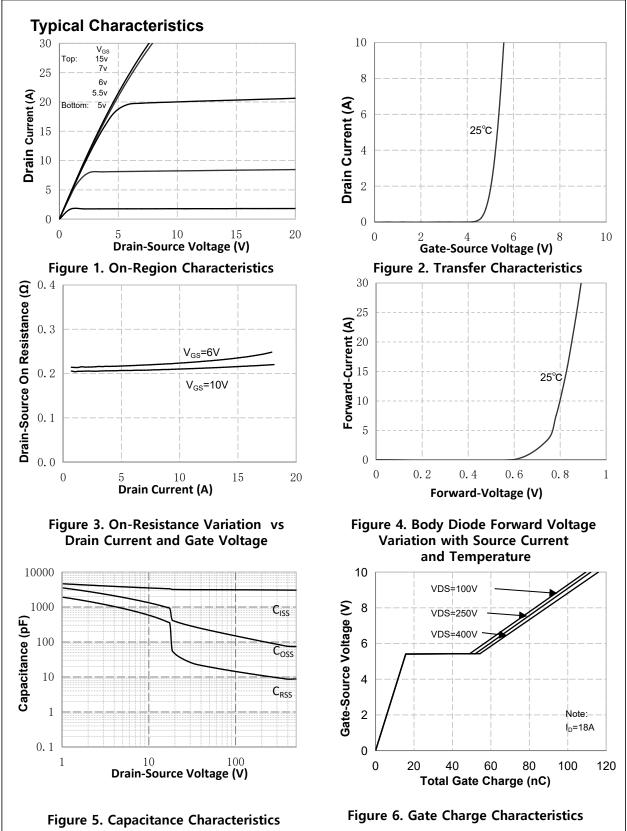
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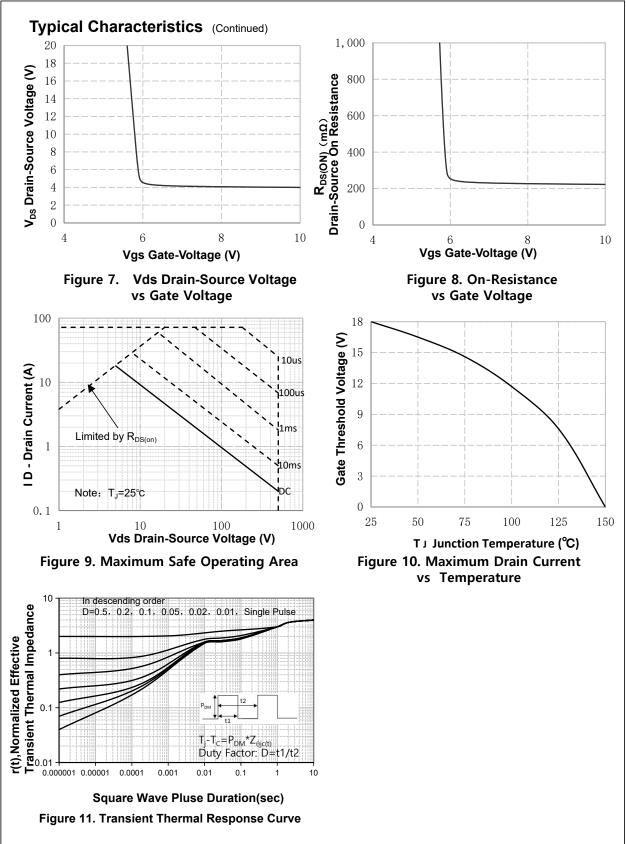
T = 25°C unloss othorwise noted

Electr	rical Characteristics T	_C = 25°C unless otherwise noted				
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Ch	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 uA	500			V
∆BV _{DSS} / ∆T _J	Breakdown Voltage Temperature Coefficient	I _D = 250 uA, Referenced to 25°C		0.59		V/°C
	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V			1	uA
I _{DSS}		V _{DS} = 400 V, T _C = 125°C			10	uA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V			-100	nA
On Cha	aracteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \text{ uA}$	3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 9A		212	265	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D =9A		12		S
Dynam	ic Characteristics		ı	II.	ı	
C _{iss}	Input Capacitance			3110		pF
Coss	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz		328		pF
Crss	Reverse Transfer Capacitance	1 - 1.0 WH 12		32		pF
Switch	ing Characteristics			•		
t _{d(on)}	Turn-On Delay Time			65		ns
t _r	Turn-On Rise Time	$V_{DD} = 250 \text{ V}, I_D = 18 \text{ A},$		40		ns
t _{d(off)}	Turn-Off Delay Time	$R_G = 25 \Omega$ (Note 4, 5)		245		ns
t _f	Turn-Off Fall Time	(Note 4, 5)		68		ns
Qq	Total Gate Charge	V _{DS} = 250 V, I _D =18A,		116		nC
Q _{gs}	Gate-Source Charge	V _{GS} = 250 V, I _D = 16A,		16		nC
Q _{qd}	Gate-Drain Charge	(Note 4, 5)		38		nC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
Is	Maximum Continuous Drain-Source Diode Forward Current				18	Α
I _{SM}	Maximum Pulsed Drain-Source Diode F	num Pulsed Drain-Source Diode Forward Current			72	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 9A			1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 18A,		525		ns
Qrr	Reverse Recovery Charge	dl _F / dt = 100 A/us (Note 4)		6.2		uC
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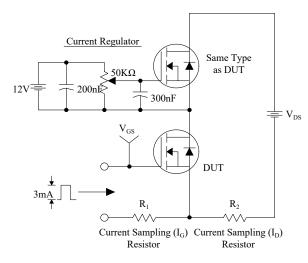
- 1. Repetitive Rating : Pulse width limited by maximum junction temperature 2. L = 0.5 mH, V_G =10V, V_{DD} =50V, Starting T_J = 25°C 3. $I_{SD} \le 20A$, $di/dt \le 200A/us$, $V_{DD} \le BV_{DSS}$, Starting T_J = 25°C 4. Pulse Test : Pulse width $\le 300us$, Duty cycle $\le 2\%$

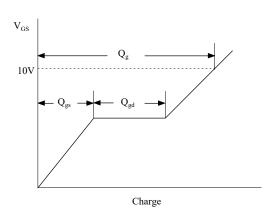
- 5. Essentially independent of operating temperature



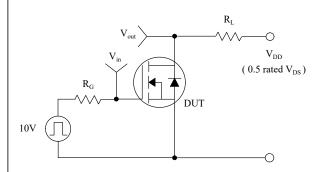


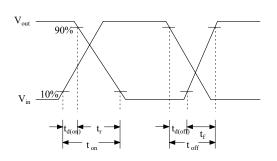
Gate Charge Test Circuit & Waveform



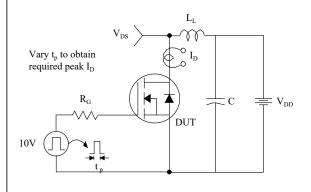


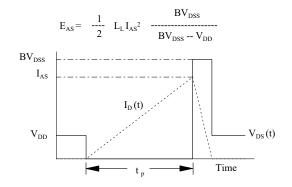
Resistive Switching Test Circuit & Waveforms



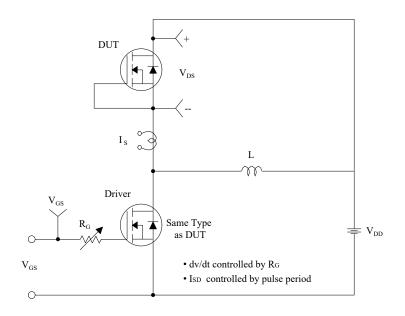


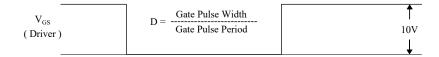
Unclamped Inductive Switching Test Circuit & Waveforms

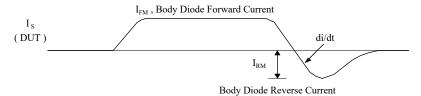


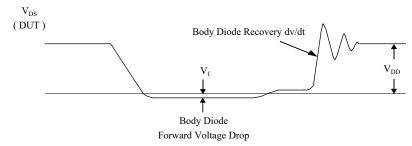


Peak Diode Recovery dv/dt Test Circuit & Waveforms

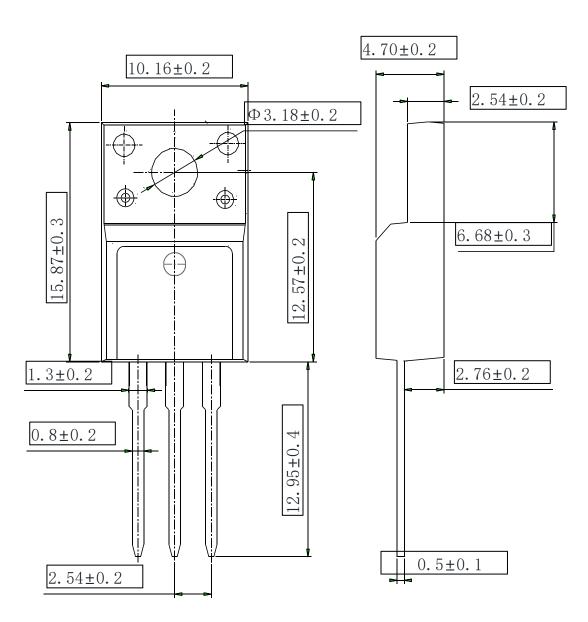








TO-220F OUTLINE



NOTE:

1The plastic package is not marked as smooth surfaceRa=0.1; Subglossy surfaceRa=0.8 2. Undeclared tolerance \pm 0.15, Unmarked filletRmax=0.25

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